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CHANGE RECORD

ISSUE	DATE	PAGE	DESCRIPTION OF CHANGES	RELEASE

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1. ACRONYMS

ADC Analog to Digital Converter
BLR Baseline Restorer
BRSB Burst chain Bus
CERN Centre Europeenne Reserches Nucleaires
DAC Digital to Analog Converter
DFEE Digital Front End Electronics
EM Electro Magnetic
FITS
FIFO First In First Out
FPGA Field Programmable Gate Array
GRID Gamma Ray Imaging Detector mode of AGILE
GSB Grid chain Bus
GUI Graphical User Interface
HC Host Computer
HK Housekeeping
I/F Interface
MCA Multi Channel Analyser
MCAL Agile Minicalorimeter
MUX Multiplexer
LLD Lower Level Discriminator
LVDS Low Voltage Drop Swing
PD PhotoDiode
PG Pulse Generator
PSU Power Supply Unit
SC Science Console
SEM Simplified Engineering Model
SW Software
TE Test Equipment
TC Telecommand
VME Versa Module Eurocard
ZCD Zero Crossing Discriminator

2. APPLICABLE AND REFERENCE DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD [1] *AGILE-DWG-SP-001 Issue 04*
AD [2] *AGILE-ITE-RE-002 Issue 1.1*

2.2 REFERENCE DOCUMENTS

RD [1] *TL17716 Issue 04*
RD [2] *TL19362 Draft*
RD [3] *AGILE-ITE-TN-005 Issue 1*

3. SEM MCAL DESCRIPTION

3.1 SEM MCAL

The SEM electronics is made of two electronics boards board X and board Z (see Figure 3.1-1 and Figure 3.1-2).
The two boards are about 400 x 400 mm in size; they have the same mechanical dimension of the MCAL detector and are designed to be stacked below it.
The boards are mounted orthogonal to each other and interconnected via the connector placed at the center of the boards.
For mechanical constraints, in the SEM, the two boards are interconnected with a cable about 50 cm long.
SEM_MCAL has been placed inside a mechanical box that has also the function of EM shield.
The bars detectors of MCAL plane X will run parallel to board X so than all the preamplifier with the signals from of sides A and B are directly faced to their correspondent analogue chains on the board. The same occurs for the bars of MCAL plane Z and board Z.

BOARD X

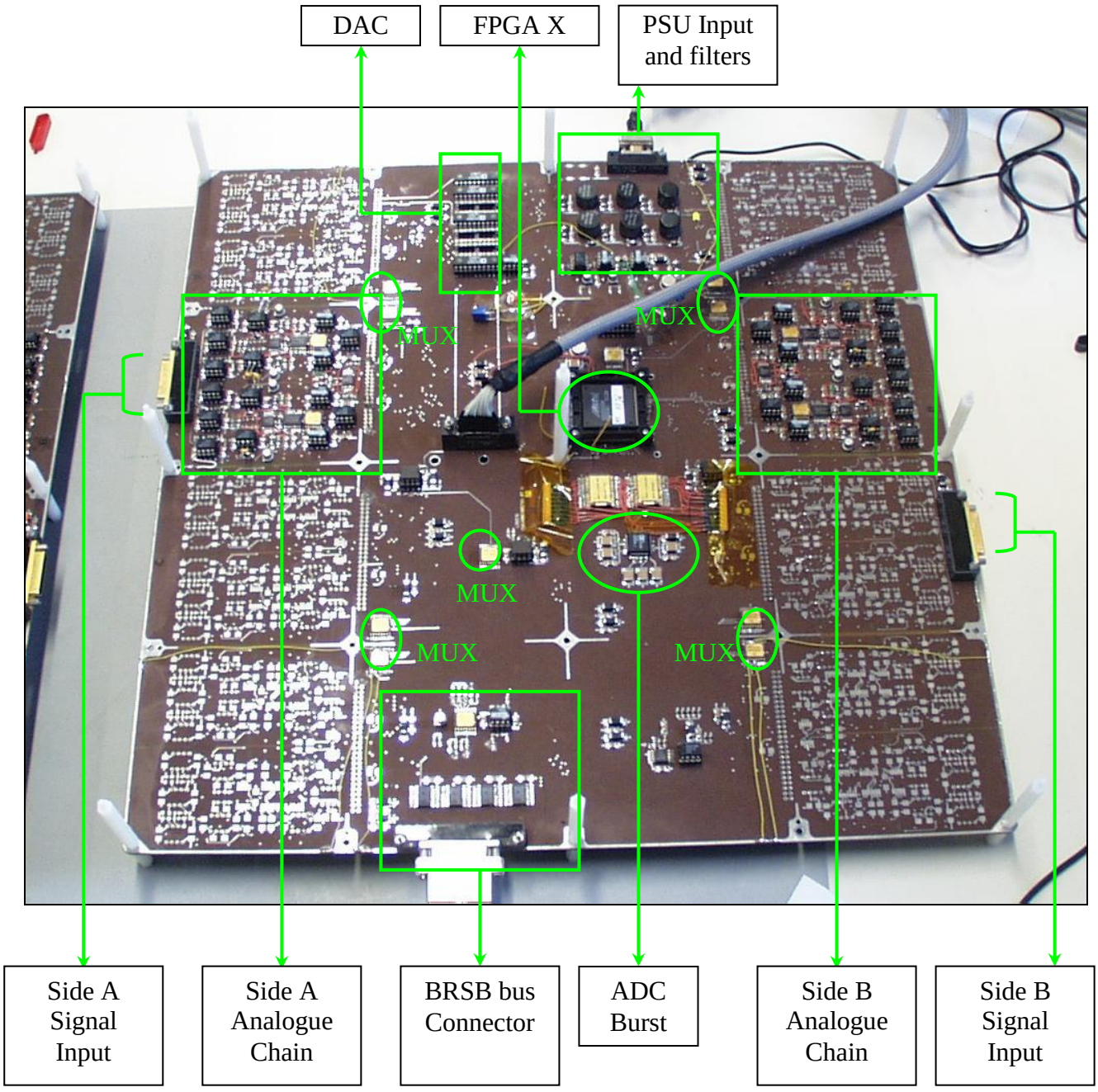

Figure 3.1-1: SEM MCAL electronic boards, board X. They are clearly visible the 8 analogue chains circuitry (side A and side B block).

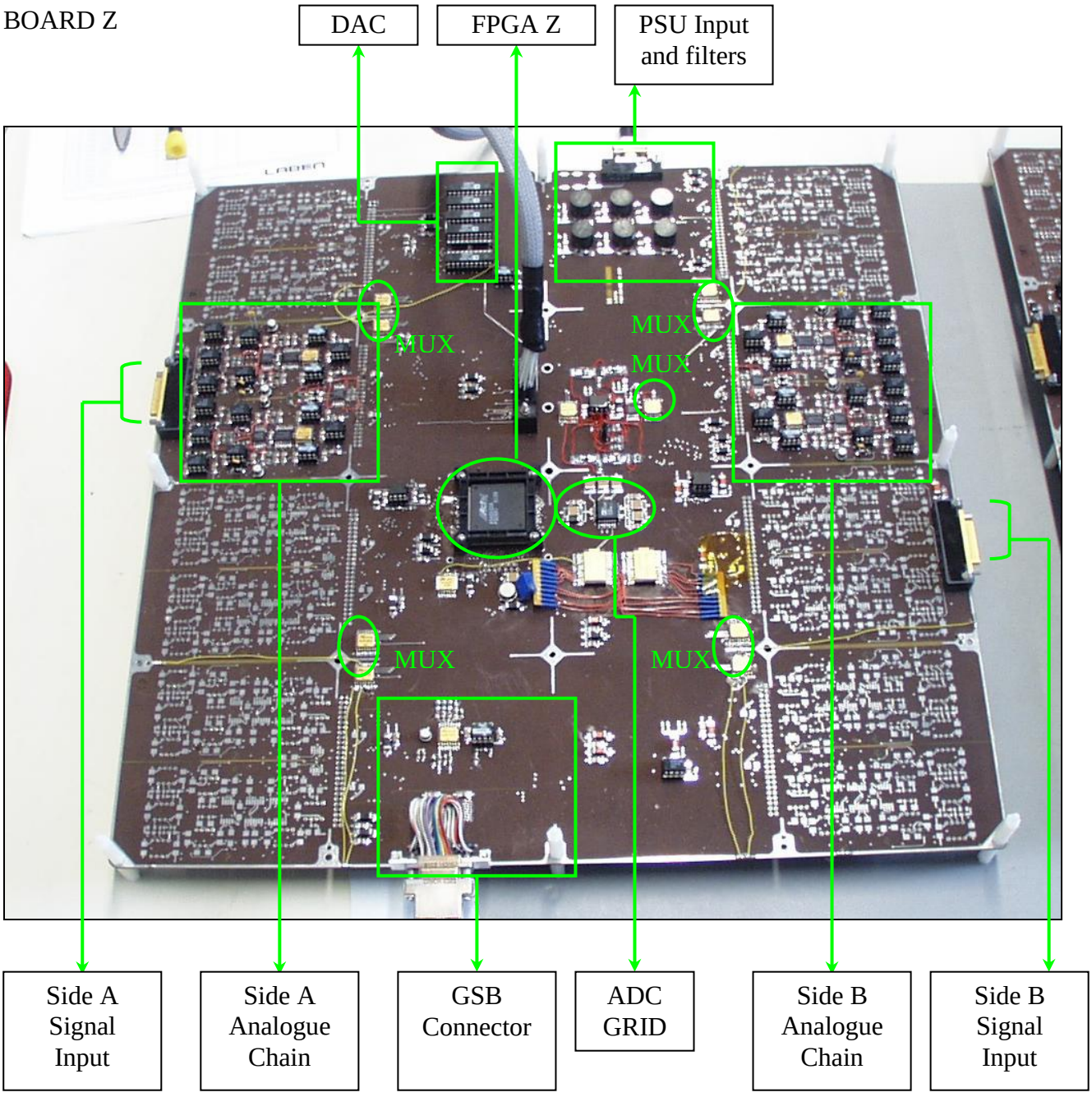

Figure 3.1-2: SEM MCAL electronic boards, board Z. They are clearly visible the 8 analogue chains circuitry (side A and side B block).

3.2 SEM MCAL FUNCTIONS

The block diagram of the MCAL SEM is depicted in Figure 3.2-1
Functionally MCAL SEM includes:

- 16 analog chains, conditioning the signals coming from the two sides of 8 bars, 4 in Board X and 4 in Board Z.
- On Board:
  - the FPGA that manages the logic for the Burst chains.
  - the MUX, ADC and FIFO to convert and temporary store the analogue signals for the Burst chains.
  - the I/F for the Burst chain.
- On Board Z:
  - the FPGA that manages the logic for the GRID chains.
  - the MUX, ADC and FIFO to convert and temporary store the analogue signals for the GRID chains
  - the I/F for the GRID chain.
- Fast trigger chain to detect high energy deposits on the whole MCAL.
- Power supply stabilization filters.
- Ratemeters to count events detected on bar sides and correspondent HK preparation.
- Logic for TC receiving and implementation.
- On Board X, the I/F for HK transmission and TC receiving.

The system can operate in two states

- IDLE events will not be processed, ratemeters are stopped, TC are received
- OBSERVATION events are processed, ratemeters work, TC are received

The design of the board is almost that of the flight model design, so it is designed to host 64 analogue chains, among which only 16 are populated with circuitry.

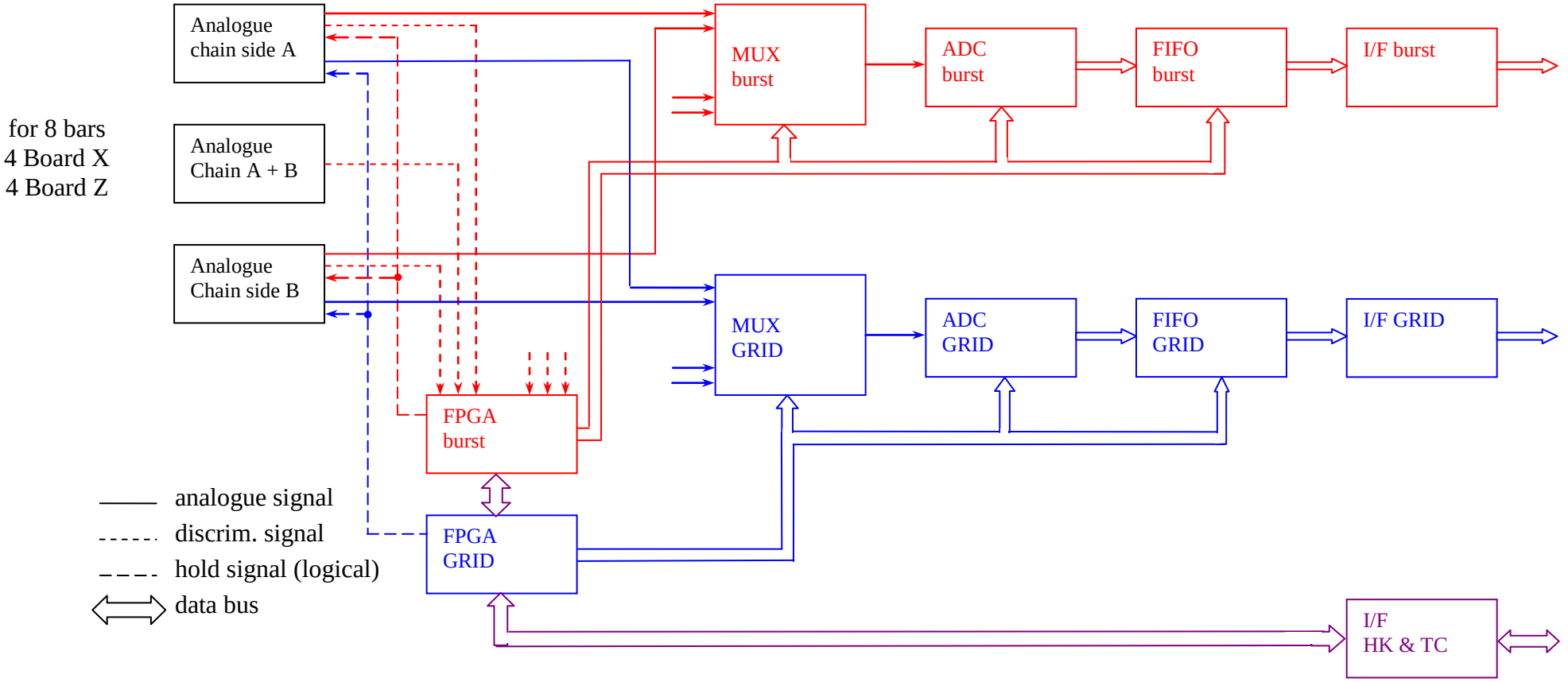

Figure 3.2-1 SEM MCAL block diagram

3.3 SEM MCAL TC AND HK

The following TC are implemented in SEM MCAL

Telecommand	Notes
Global system reset	
System state change	From IDLE to OBSERVATION
Reset Burst FIFO	
Reset GRID FIFO	
State register reading	
Enable – Disable bars	Allows to disable the effect of the selected bar triggers on the burst chain.
Set THR base	Allows to define a common value for all the threshold that will be tuned later with individual values.
Set THR in the burst chain for each bar PD and for each bar PD sum	Fine threshold setting for each trigger circuit
Set fixed ratemeter pointer	Allows to define which ratemeter will be refreshed with 16 sec period
Delay GRID	In GRID mode set the delay between the external T1_YES signal and the hold of analogue chains

Table 3.3-1 SEM TC implemented

The following TC are NOT implemented in the SEM

Telecommand	Notes
Set THR fast	Allows to set the threshold for the fast branch
Select width of multiple events coincidence	Allows to select the width of the time window considering coincident events coming from different bars.
Send calibration signals	Allow to send electrical calibration signal to pre-amp inputs

Table 3.3-2 SEM TC not implemented

The following HK are supplied by the SEM

HouseKeeping	Notes
Ratemeters board X	Ratemeters of the burst chain triggers (for each bar: side A, side B, sum A+B). A value is refreshed every 240 sec
Ratemeters board Z	Ratemeters of the burst chain triggers (for each bar: side A, side B, sum A+B). A value is refreshed every 240 sec
Fixed ratemeter board X	One of the above mentioned ratemeters of board X selected to be refreshed every 16 sec
Fixed ratemeter board Z	One of the above mentioned ratemeters of board Z selected to be refreshed every 16 sec

Table 3.3-3 SEM Digital HK implemented

The following HK are not supplied by the SEM

HouseKeeping	Notes
Live time meter of the Burst chain	
Live time meter of the GRID chain	
Fast Ratemeters	Ratemeters of the fast chain.
Voltages	Analogues HK
Temperatures	Analogues HK

Table 3.3-4 SEM HK not implemented

3.4 SEM MCAL CONNECTORS

The connectors of the two boards are the following (see Appendix A for pin function):

Board X
- 1 PSU connector
- 1 Burst connector
- 1 Pre-amp side A plane X connector
- 1 Pre-amp side B plane X connector

Board Z
- 1 PSU connector
- 1 GRID connector
- 1 Pre-amp side A plane Z connector
- 1 Pre-amp side B plane Z connector

3.5 SEM MCAL ANALOGUE CHAIN FUNCTIONS

In Figure 3.5-1 is depicted the block diagram of an analogue channel of the SEM

Both GRID and Burst chains have in common the amplification and shaping block.

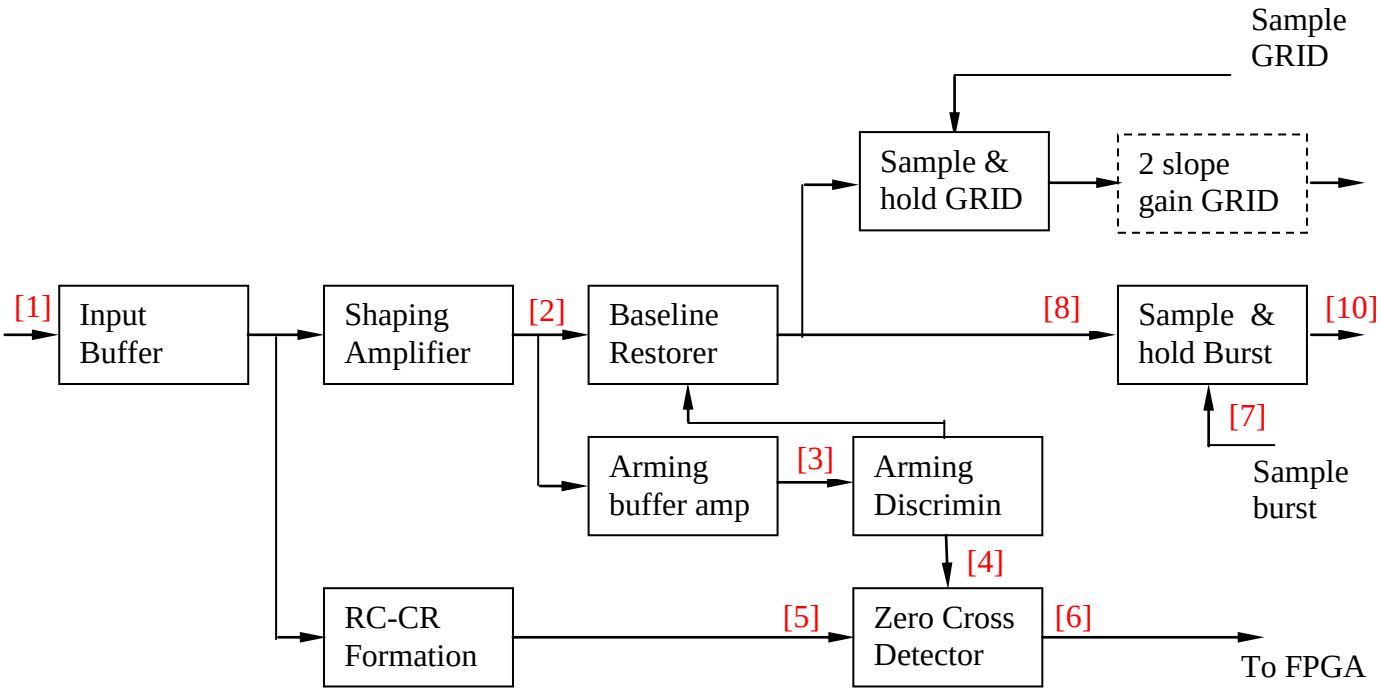

Figure 3.5-1 Block diagram of one analogue chain. The input is connected to a PD pre-amplifier. The signals in the different points are indicated by numbers inside brackets.

3.6 SEM MCAL BURST CHAIN

The Burst chain is able to self generate the command to sample and convert the signals above the noise of the bars.

The data stream has the structure described in Table 3.6-1. The protocol of data transmission is described in Figure 3.6-1
MCAL can send stream of data concerning one bar (single event) or more bar (multiple events); multiple events are coincident events generated by the same precursor physical interaction in more than one bar. Event are considered coincident when they occour inside a time window whose width is selectable via TC.
The functional beahviour of the various block of the Burst chain is described in Figure 3.6-2; the input stimulus has been generated with a pulse generator and the waveforms has been take with a scope triggered by the pulse generator; the amplitudes of the waveforms has been normalised and does not correspond to the real values.

The input signal (point [1] of Figure 3.5-1) is injected, via a buffer, into the shaping amplifier, whose output [2] is feed into
- A baseline restorer block followed by the sample and holds circuits.
- The arming discriminator block.

In the arming discrimination block the shaped signal is first amplified for a factor of 50 and clamped [3] then compared with a threshold level to generate the arming signal [4] to enable the Zero Crossing detection block.
The Zero Crossing detection block amplifies, differentates and clamps the input signal [5]; then, if enabled by the arming discriminator, generates a logical signal almost in corrispondence of the signal peak from the Shaping Amplifier [6] that is sent to the FPGA for logical processing.
The logic in the FPGA generates the sample signal [7] that is used in the sample and hold block to sample the shaped signal [8] to fed the MUX and ADC block with a stable signal [10].
The logic to generate a burst hold for a bar is described in Figure 3.6-3.
A sample burst signal is generated if one of the bar discriminators (bar side A, bar side B, side A+ side B) fires and the bar is active.
The sample signal activate the holding in the sample and hold block. There is a little delay between the peaking time of the strectched signal out of the analogue chain and the peaking time of the signal of the sample and hold; this delay is of the order of 2 μsec and is long enough so than the stretching occours at the maximum of the peak.
The stretched signal is fed into a Multiplexer whose output [11] feed the ADC. For every bar there is alwais a conversion of both sides A and B.
The FPGA logic generates also a BSRB_Timing [13] logical signal that is sent to AGILE DH (or SEM-MCAL TE). This signal is used by these devices to associate a time marking to the event. It will be a task of the devices receiving the burst data to build a data stream that for each event include also the timing. Just one BSRB_Timing signal is generated both for single and multiple events.

Burst data generation follows Analogue to Digital conversion of the bars signal amplitudes.
Burst data have the format described in Table 3.6-1.
This format is generated in the FPGA, stored in Burst FIFO and transmitted via the BSBR bus with the timing described in Figure 3.6-1
Data are transmitted to the external with LVDS levels.

MSB																LSB
b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	B6	b5	b4	b3	b2	B1	b0
Bar counter (5 bits)					Side A energy (12 bits)											
Bar address (5 bits)					Side B energy (12 bits)											

Table 3.6-1: Structure of data on the BRSB_DATA_DWN line (34 bits)

Bar counter: **5 bit field**
When a single event is detected this filed is 0.
When a multiple event is detected (one event with multiple bars triggered and the same time tag) this field contains the value 31 at first, and then decreases as the bars data is read.
When the data of the last bar is transferred this field jumps to 0.
Example of the Bar Counter for a 3 bars events: 31→30→0
Bar address: **A 5 bits field that indicates the address of the bar triggered.**
Side A/B energy: **12 bit field, is the digitally converted value of the analogue signal read on each bar's PD (side A and B)**

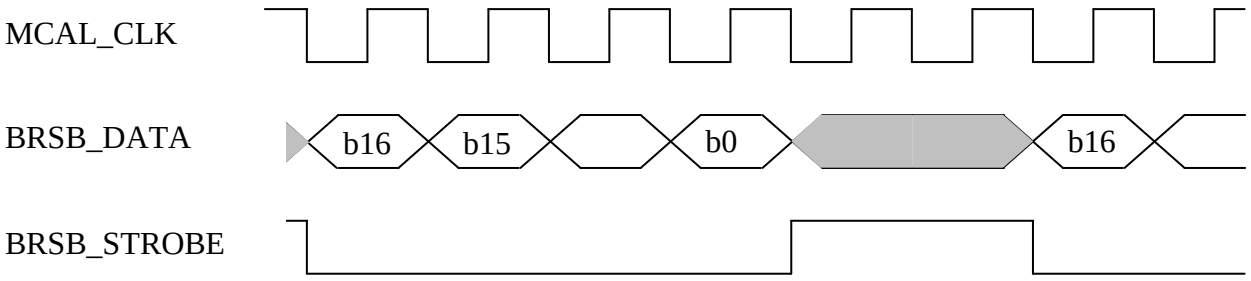

Figure 3.6-1 Timing of BSRB bus. Notice that between two valid strobe signal there is one clock pulse if the strobe separates data describing the two PD of the same bar, while there are two clock pulses if the strobe separates data coming from different bars.

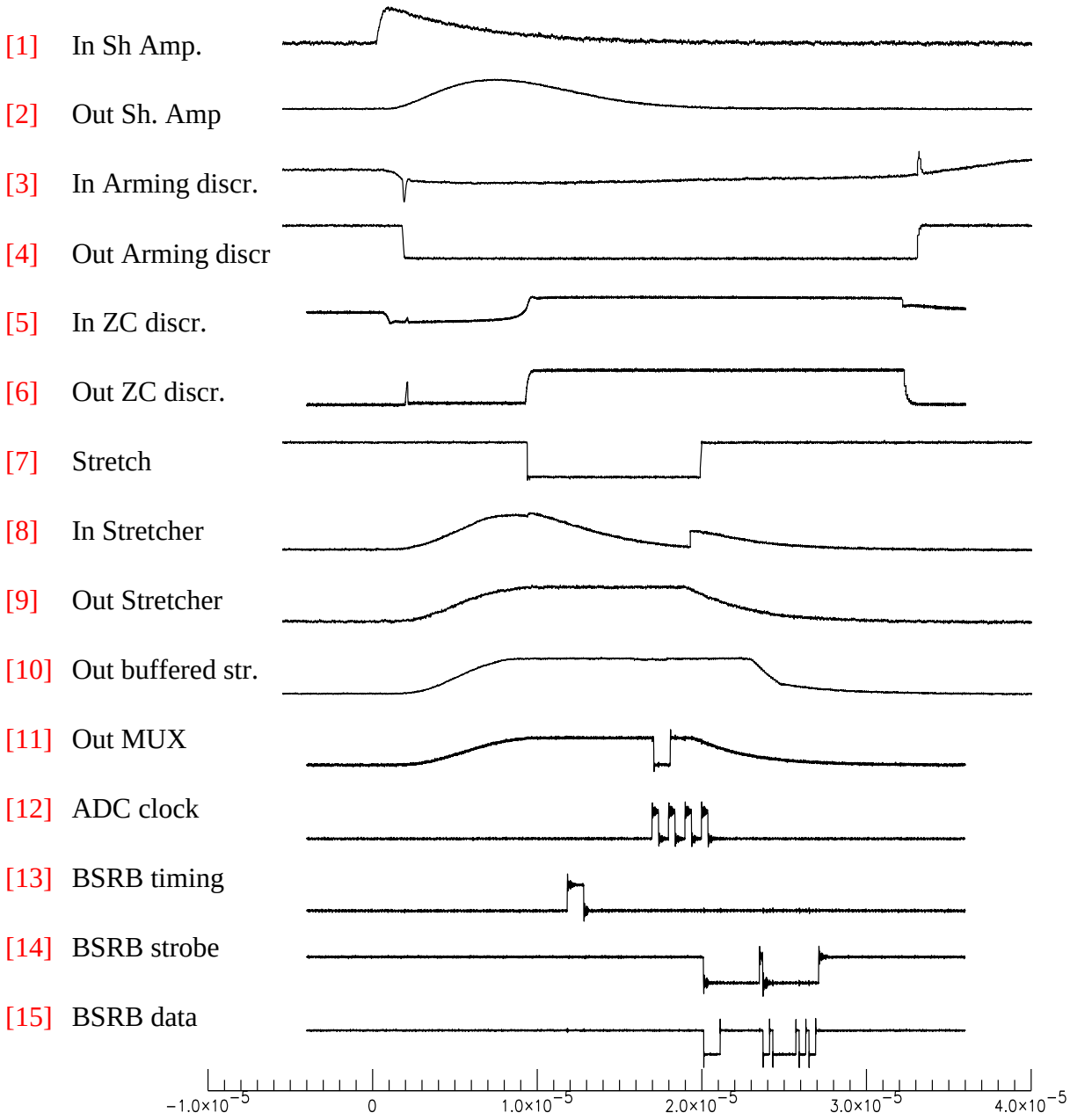

Figure 3.6-2 Waveforms of the signals, taken with the oscilloscope. The x axis is in sec. Channel 5A has been stimulated with a pulser. The amplitudes has been normalised.

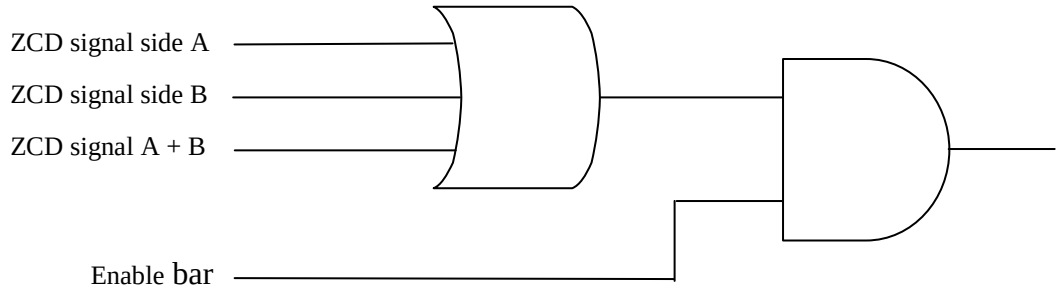

Figure 3.6-3 Burst logic generation for a bar

3.7 SEM MCAL GRID CHAIN

The analogue chain for the GRID is in common with the Burst chain up to the stretcher unit.
At this point another stretcher is used; it is commanded by an hold signal from the FPGA (GRID_HOLD) related to an external command signal T1_YES (see Figure 3.7-2) .
Upon arrival of the GRID_HOLD signal the shaped signal of the analogue chain is stretched and sent to the multiplexer, and finally to the ADC via a last amplifying stage that allows to select the GRID energy range. This has not been implemented in the SEM MCAL.
When the GRID_HOLD signal is issued both side for all the bars whatever is the content of their analogue chain is sampled and converted. This logic is managed by the FPGA GRID.
The delay between the external T1_YES signal and the GRID_HOLD shold be long enough so to reach the maximum of the signal. This delay can be set by TC.

The output data stream format of the GRID chain is depicted in Table 3.7-1
Data are transmitted to the external with LVDS levels with the protocol described in Figure 3.7-1 always all the 60 bar data are transmitted.

MSB											LSB
b11	b10	b9	b8	B7	b6	b5	b4	b3	b2	b1	b0
Bar 0 Side A energy (12 bits)											
Bar 0 Side B energy (12 bits)											
…											
Bar 29 Side A energy (12 bits)											
Bar 29 Side B energy (12 bits)											

Table 3.7-1MCAL GRID data stream format

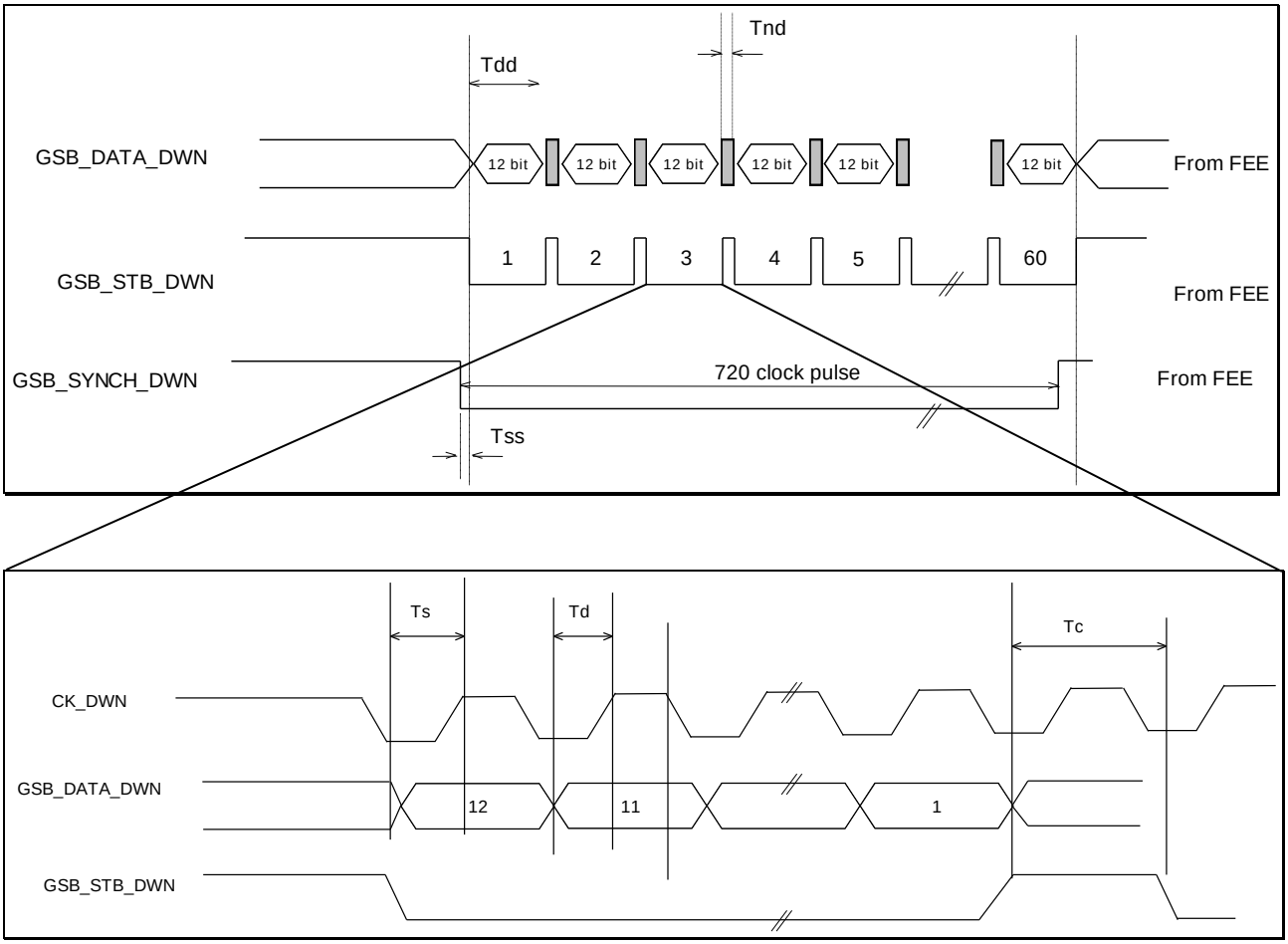

Figure 3.7-1 GRID Board signals timing

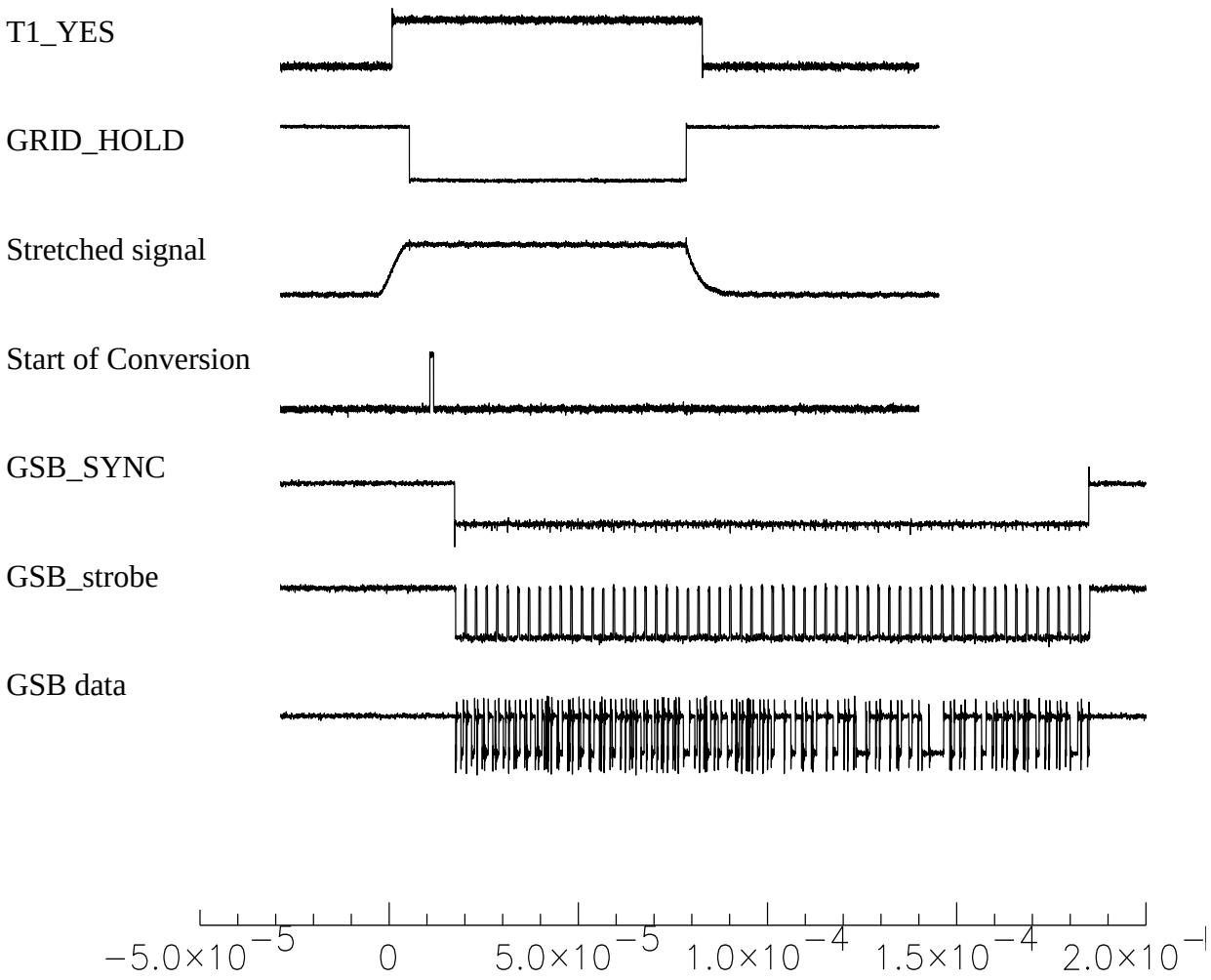

Figure 3.7-2 Waveforms of the signals, taken with the oscilloscope, for the Channel 5 on the GRID Chain. The amplitudes has been normalised . The input signal is generated with a pulse generator as well as the T1_YES.

4. TEST SYSTEM SET-UP

SEM-MCAL was tested both with standard laboratory equipment and with a dedicated SEM-MCAL test equipment.
The first configuration was mainly used to test independently the various circuital blocks of SEM-MCAL.
The TE was mainly used to test SEM-MCAL as an overall system.
As a stimulus to the system were used or electronic pulser, or radioactive sources or finally beams of energetic particles and photons, depending by the objective of the test.

4.1 STANDARD LABORATORY EQUIPMENTS

In Figure 4.1-1 is schematically represented the configuration used to test SEM-MCAL with standard laboratory equipments.
Some time the pulser was used or directly to inject a pulse with defined amplitude at the SEM-MCAL input.
In different configuration the pulser was used to inject a charge, via a calibrated capacitor, at the input of the Pre-amplifiers of a representative model of the CsI(Tl) bars.

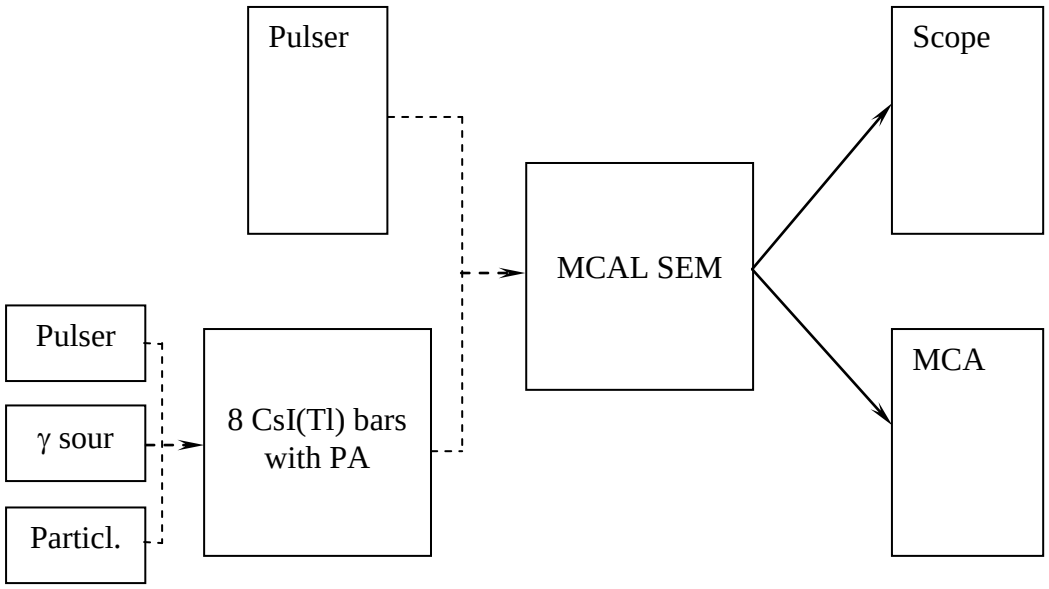

Figure 4.1-1 Configuration of the SEM-MCAL for test with standard laboratory equipments.

4.2 SEM-MCAL TEST EQUIPMENT

Its function is to provide support for testing, calibration and monitoring of the SEM-MCAL instrument as a system.

- The Test Equipment includes (Figure 4.2-1):

- A VME crate that allow to interface the the MCAL-SEM to Host Computer

- The Host Computer (HC) that should:
  - Obtain data from the instruments
  - Generate a pseudo-ESA telemetry packet corresponding to the start/stop event of an acquisition.
  - Forward to the Science Console the raw data and the start/stop TC packet by means of a TCP/IP connection.

- A Science Console (SC) that has the task of:
  - Receive the TM and TC packets sent by the HC.
  - Store the raw data in the raw format and with a description of each measurement.
  - Convert the raw data in FITS format.
  - Provide a Quick Look functionality of acquired data.

In the VME-system, each MCAL-SEM interface is connected to a dedicated board. The boards in the VME system are:

- the GRID board, for the GRID acquisition chain, that reads the SEM-MCAL events in MCAL GRID mode. In this case the SEM-MCAL needs an external trigger to start the acquisition (T1_YES signal).
- the Burst board, for the Burst acquisition chain, that reads the SEM-MCAL events in MCAL Burst mode. The generation of Burst events is autonomously decided inside the SEM-MCAL.
- the HK-Conf board, for the HK acquisition and for commanding of SEM-MCAL
- the bridge board that handles the communication between the VME system and the host computer. (
- Figure 4.2-1) used with the TE of the AGILE-ST for common tests.

The TE SW allows to:

- Configure the SEM via TC
- Start/Stop Burst acquisition
- Start/Stop GRID acquisition
- Start/Stop Digital HK acquisition
- Connect the HC

- Send data to HC
- Have a real time quick look of the data on HC
- Save data (GRID, Burst, HK) on HC
- Process and display data acquired on HC

The main commands of TE SW are reported in Appendix B

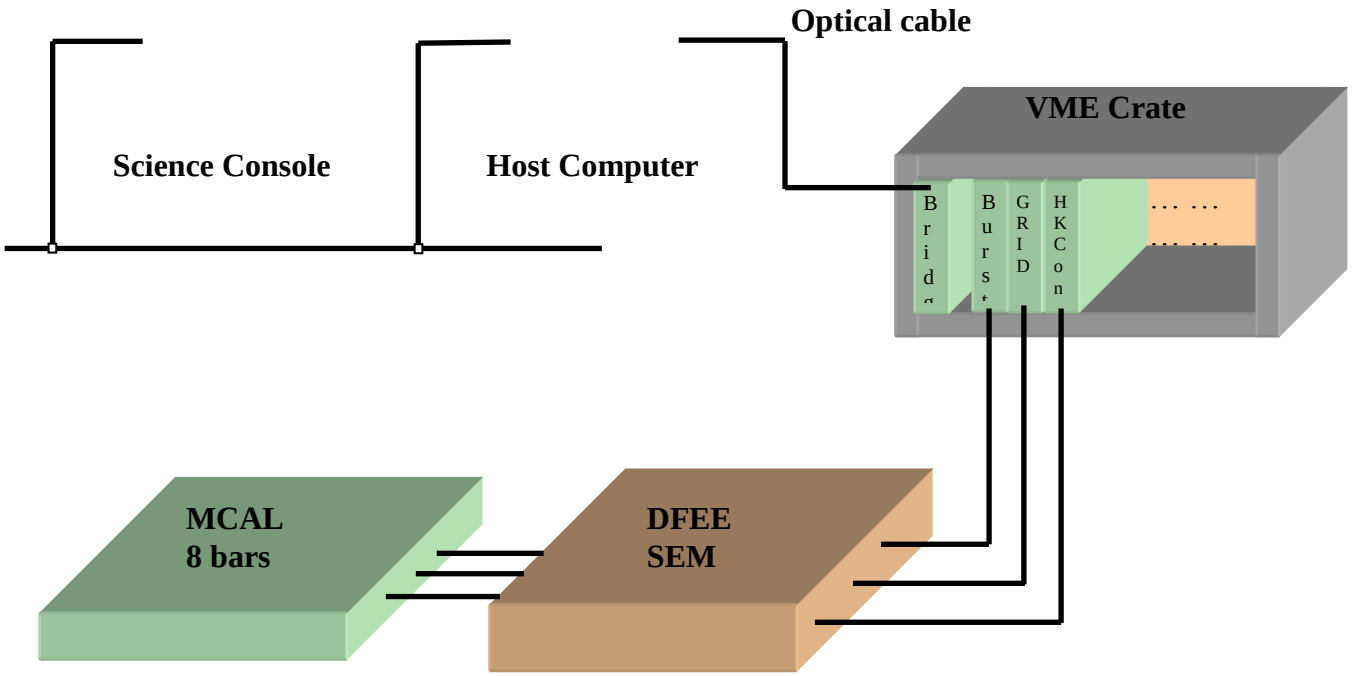

Figure 4.2-1 SEM MCAL Test Equipment set up

Figure 4.2-2 SEM MCAL Test Equipment

5. MCAL SEM FUNCTIONAL TEST

5.1 FUNCTIONAL TEST FLUX

In the following are reported details of the SEM function tested. The test were done with the aim of gaining confidence with the details of the MCAL electronics.
The flux of the SEM-MCAL test is depicted in Figure 5.1-1

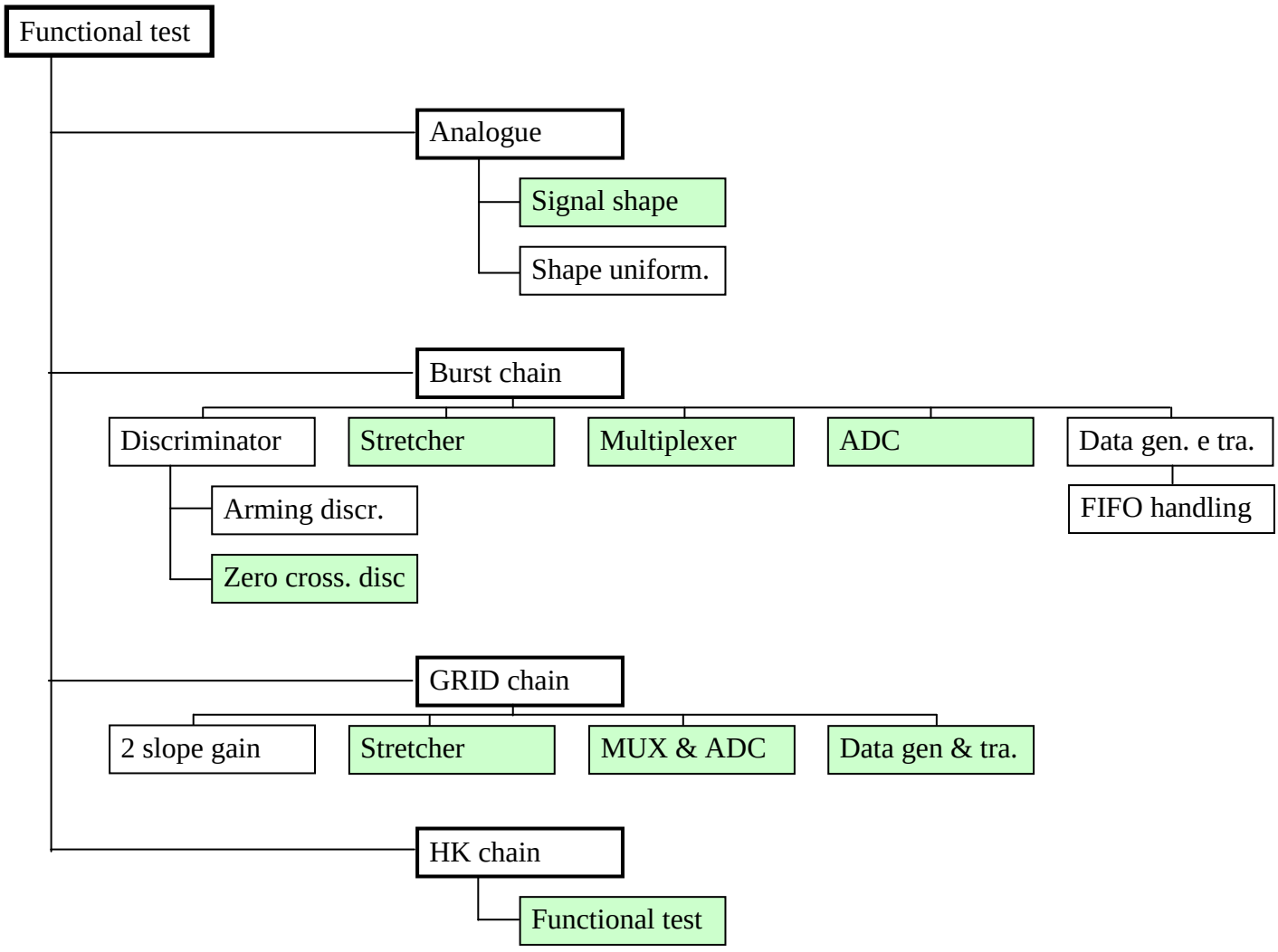

Figure 5.1-1 Functional test flux: green box indicate good behaviour.

5.2 SIGNAL SHAPING IN THE ANALOGUE CHAIN

The first stage of the analogue chain amplifies the signals coming from the PD on one of the bar sides through a charge preamplifier and applies a shaping filter. Peaking time of the shaped pulse is ~ 6 μs. After the signal shaping a Baseline Restorer keeps the baseline of the signal at a constant level.

Channel 5A has been tested:

Input signal from Pulser BNC DB-2 directly connected to SEM_MCAL input with a 50 Ohm load to ground:

Amplitude	1	V
Rise Time	0.5	μsec
Fall Time	50	μsec
Frequency	9	Hz

Figure 5.2-1 shows the Shaping Amplifier behavior. The stage works correctly

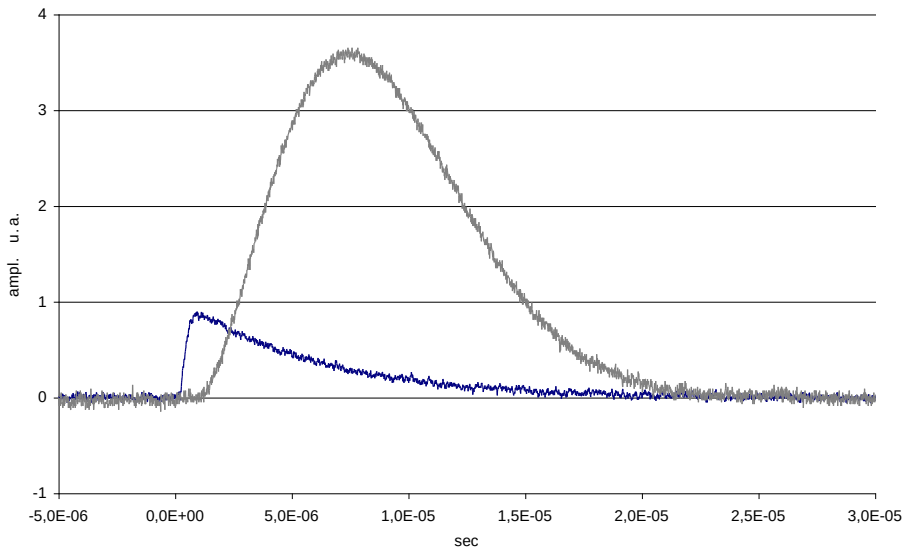

Figure 5.2-1: Pulse generated by Pulse Generator as seen on channel 5A input (IC U201A pin 3) and output (IC U202A pin 1).

5.3 PULSE SHAPE UNIFORMITY ON THE VARIOUS CHANNELS

Channel tested: Board X 5A, 6A, 7A, 8A, 8B
Board Z 5A, 6A, 7A, 8A, 8B

Input signal from Pulser BNC DB-2 directly connected to SEM_MCAL input with a 50 Ohm load to ground:

Amplitude	1	V
Rise Time	0.5	µsec
Fall Time	50	µsec
Frequency	9	Hz

The two shapes detected are shown in Figure 5.3-1 :
Shape 1: Found on channels 5A, 6A, 7A, 8A, 8B of BOARD X and 5A of BOARD Z.
Shape 2: Found on channels 6A, 7A, 8A and 8B of BOARD Z.

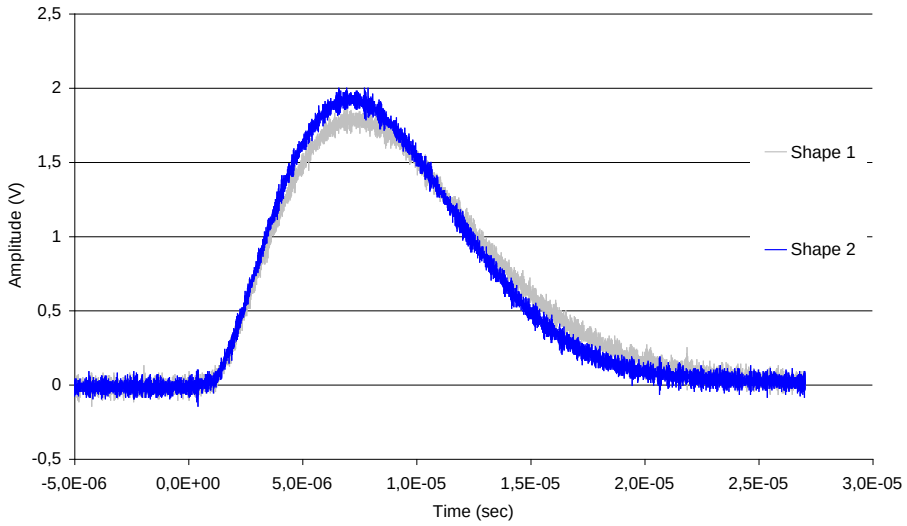

Figure 5.3-1 Two slightly different shapes detected on different analogue channels.

5.4 BURST CHAIN DISCRIMINATOR

In the Burst chain, the signal discrimination stage is composed of two parts:

- Arming discriminator: If a signal is detected over threshold it enables the ZCD circuit.
- Zero Crossing Discriminator (ZCD): Detects the top of the shaped signal. The signal in input is formed with a RC-CR net and a logical signal is generated and sent to FPGA over its zero crossing occurrence.

Channel tested: Board X 5A,

Input signal from Pulser BNC DB-2 directly connected to SEM_MCAL input with a 50 Ohm load to ground:

Amplitude	1	V
Rise Time	0.5	μsec
Fall Time	50	μsec
Frequency	9	Hz

Discr. Amplitude variable

Figure 5.4-1 shows the arming discriminator signals

Figure 5.4-2 shows the Zero Crossing Discriminator signals.

As shown in Figure 5.4-3 the length of the discriminator logical output depends on the thr value.

The behavior of the Burst chain discriminator has been found problematic when setting the threshold value to a low level.
As depicted in Figure 3.5-1 the output of the shaping amplifier is into the arming discriminator via an arming buffer amplifier (point [3] of Figure 3.6-2) where is compared with the discriminator level (Figure 5.4-1).

In order to have the arming discriminator running correctly, it should never happen that the discriminator level is below the baseline of the signal at the output of the arming buffer amplifier.
In order to detect the lower signals the discriminator level should have a value of the order of:

$V_{thr\text{-}min} > V_{arm\text{-}amp\text{-}bl} + 5*N_{arm\text{-}amp}$

Where:

$V_{thr\text{-}min}$	is the minimum threshold value
$V_{arm\text{-}amp\text{-}bl}$	is the baseline voltage at the arming amplifier buffer output
$N_{arm\text{-}amp}$	is the noise rms at the arming amplifier buffer output

It has been noticed that setting the threshold values at low levels it may happen that $V_{arm\text{-}amp\text{-}bl}$ i.e. the baseline voltage at the arming amplifier buffer output it not stable and moves for long periods (up to 3 msec) to a value above the threshold value settled causing the hanging of the whole Burst system.

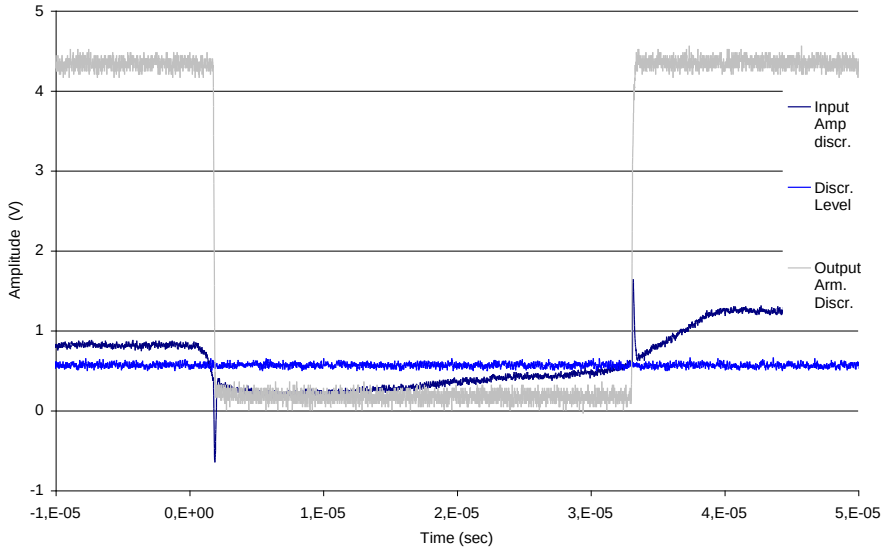

Figure 5.4-1 **Arming discriminator: Threshold level (track 1, U204A-6) and signal to be discriminated for arming (track 2, U204A-7) Signal in output from Arming Discriminator (U204A-1). The shaped signal is amplified about 50 and clamped before entering into the arming discriminator.**

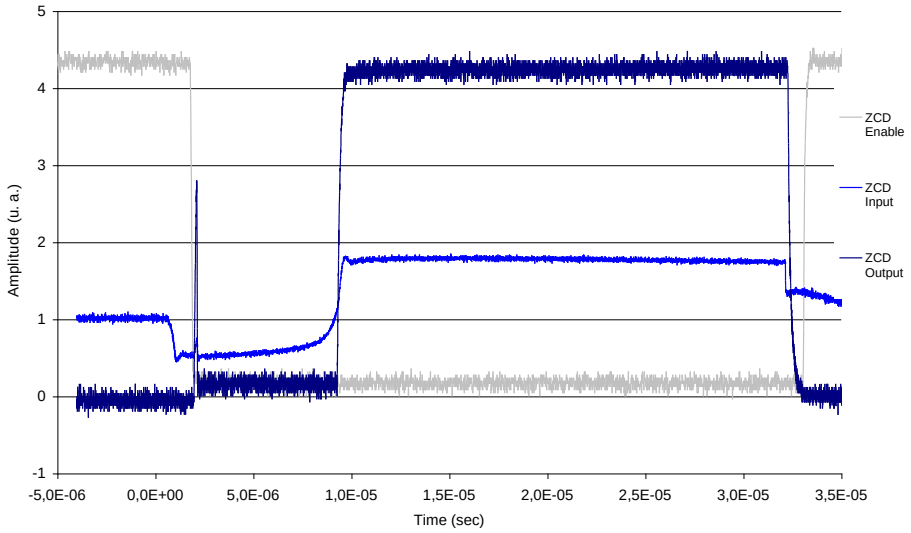

Figure 5.4-2 **Zero Crossing Discriminator input and output signals.**
CH2 is the differentiated input signal ZCD Enable: IC U207A pin 3
ZCD input (differentiate signal): IC U207A pin 4
ZCD output: IC U207A pin 1

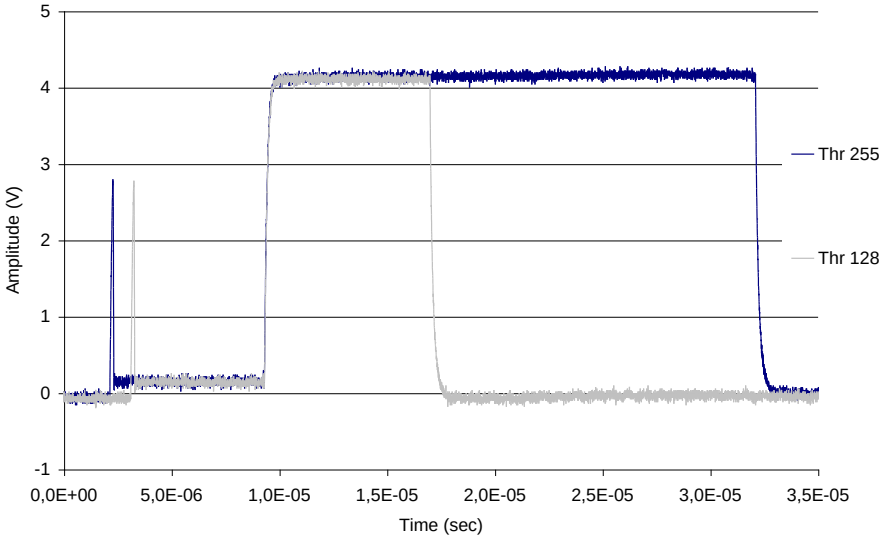

Figure 5.4-3 Length of the logical signal output from Zero Crossing Discriminator vs the threshold setting value

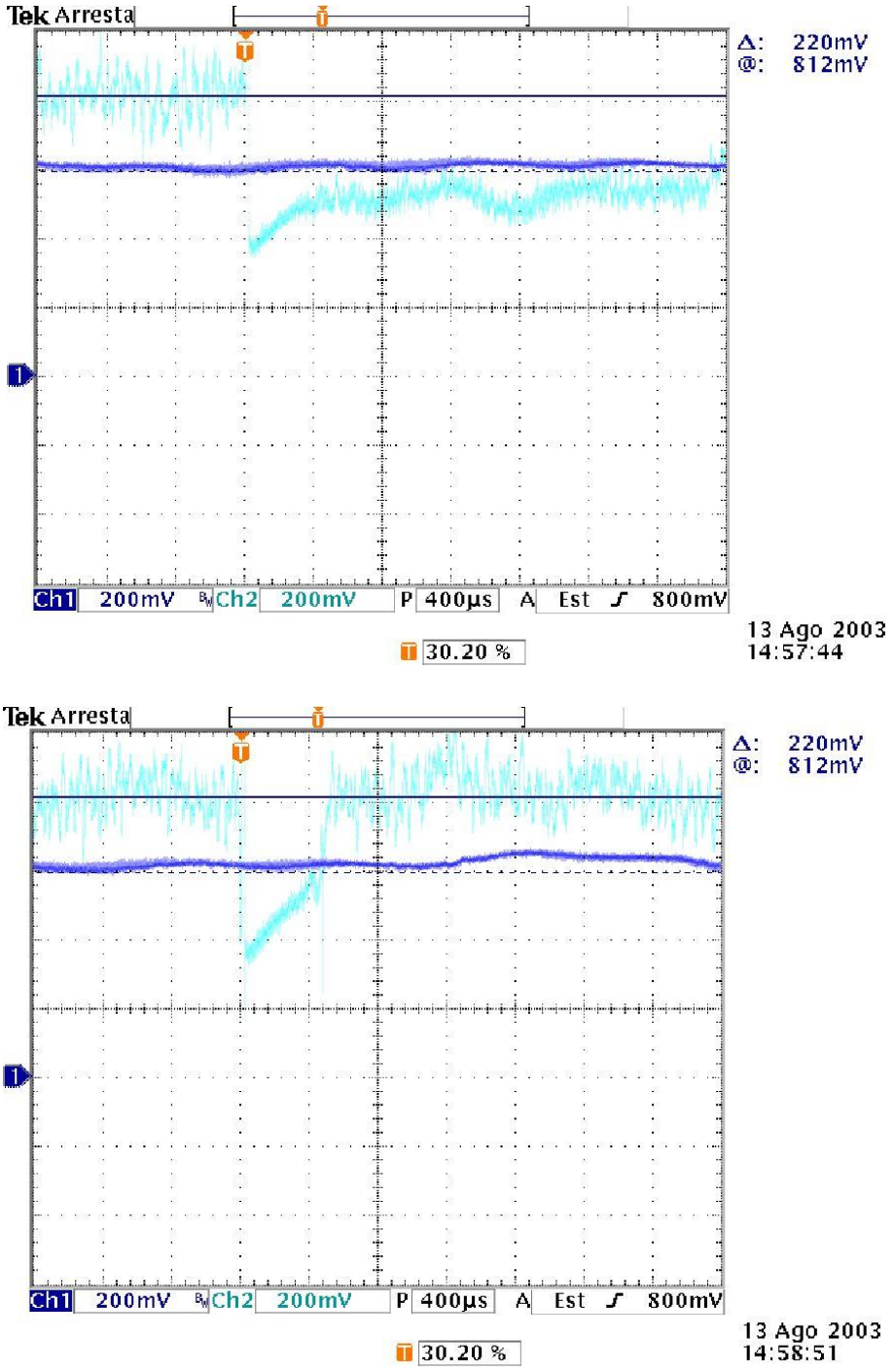

Figure 5.4-4 Effect of the baseline moving. In both pictures ch1 is the level of threshold well above the noise and ch2 id the output of the BLR circuit. The 0 voltage reference is indicated with a blue arrow with one 1 inside. The BLR circuit has an offset of 812 mV. The threshold is 220 mV below this offset.

5.5 SIGNAL STRETCHING ON THE BURST CHAIN

Channel tested: Board X 5A,

Input signal from Pulser BNC DB-2 directly connected to SEM_MCAL input with a 50 Ohm load to ground:

Amplitude	1	V
Rise Time	0.5	μsec
Fall Time	50	μsec
Frequency	9	Hz

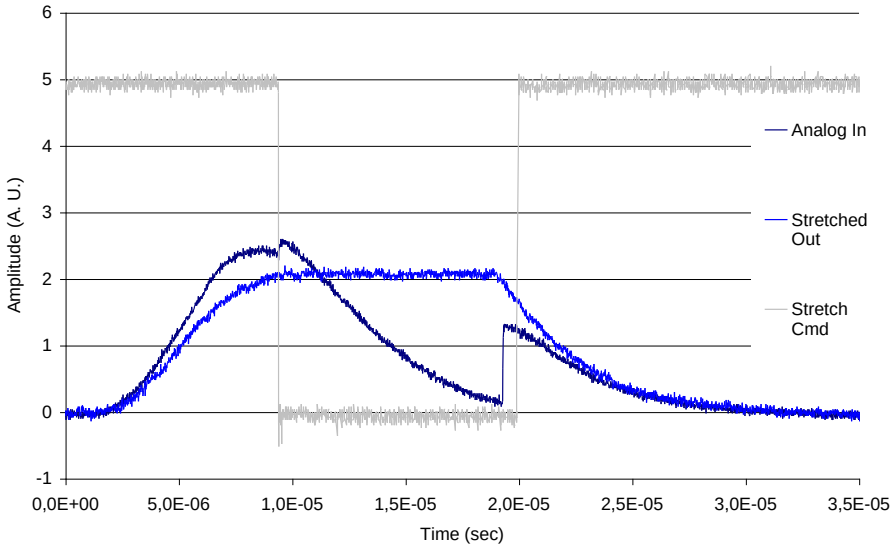

Figure 5.5-1: BURST Hold signal from FPGA (track 1) IC U205A pin 5, shaped signal (track 2) IC U205A pin 4 and stretched signal (track 3) U205A pin 1.

As depicted in

Figure 5.5-1, the stretching of the shaped signal occurs on the falling edge of the Burst Hold signal that is generated by the FPGA logic triggered by the ZCD pulses of the bars.
The Burst Hold occurs with a delay t ≅ 9.20 μs with respect to the input pulse.
The shaped signal is stretched for ~10μs depending on the Busy time of the ADC and Burst-FIFO.
Notice that the signal in output from the shaper peaks ~7μs after the pulse has been generated by PG, while the shaped pulse at the input of the stretcher peaks after ~9μs, exactly when the BURST_HOLD signal from FPGA occurs.

Notice also that the BURST Hold signal from FPGA is generated only if the SEM FIFO is not half full and the SEM is in observation mode. If the SEM FIFO gets half full the data acquisition is suspended and no more BURST Hold signals are generated.

5.6 MULTIPLEXER AND ADC ON THE BURST CHAIN

For the Burst chain there is an unique ADC; the stretched signals from the channels are multiplexed to the ADC.
There are 3 Multiplex chip on the board X and 2 on the board Z.

The multiplexing of the burst signals are done with the following scheme:

Inputs Mux 1 board X:	from 1A to 15A of this board
Inputs Mux 2 board X:	from 1B to 15B of this board
Inputs Mux 1 board Z:	from 1A to 15A of this board
Inputs Mux 2 board Z:	from 1B to 15B of this board
Inputs Mux 3 board X	connected to the Outputs of Mux1 boardX, Mux2 board X, Mux1 boardZ, Mux2 boardZ

In Figure 5.6-1 are shown the signal at the output of the MUX and the ADC clock when just one side of one bar is stimulated (ch 5A)
For every bar which has signal above at least one of the three thresholds (side A, OR side B OR SUM) signal from both sides are converted. There are always ADC two clock pulses to stop the conversion of whatever number of bars, plus two clock pulses for each bar (one for each bar side).

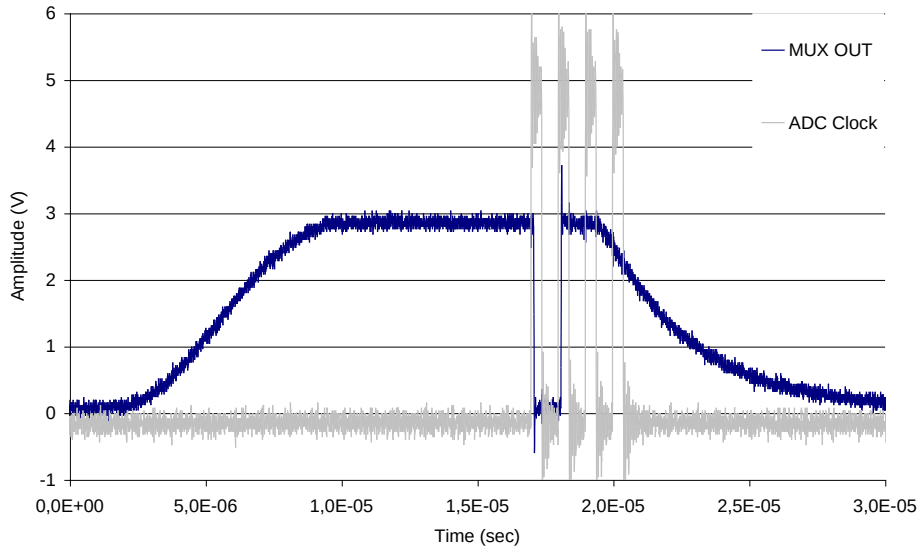

Figure 5.6-1 Mux output (IC 36 pin 4) and ADC_Clock The input signal to the multiplexing chain corresponds to the stretched signal in output from the analogue chain

5.7 BURST DATA GENERATION AND TRANSMISSION

Burst data generation follows Analogue to Digital conversion of the bars signal amplitudes.
Burst data have the format described in 3.6.This format is generated in the FPGA, stored in Burst FIFO and transmitted via the BRSB bus with the timing described in Figure 5.7-1
Data are transmitted to the external with LVDS levels.

Channel tested: Board X 5A directly connected to SEM_MCAL input with a 50 Ohm load to ground

Input signal from Pulser BNC DB-2:

Amplitude	444 and 5	mV
Rise Time	0.5	µsec
Fall Time	50	µsec
Frequency	9	Hz

Figure 5.7-1 reports the timing of the Burst bus
Although the sequence of data generation and transmission is correct, it will be seen later (paragraph 6.9), when describing the performances test that not all the channels are served with the same priority and there are bar whose events are converted with more frequency.

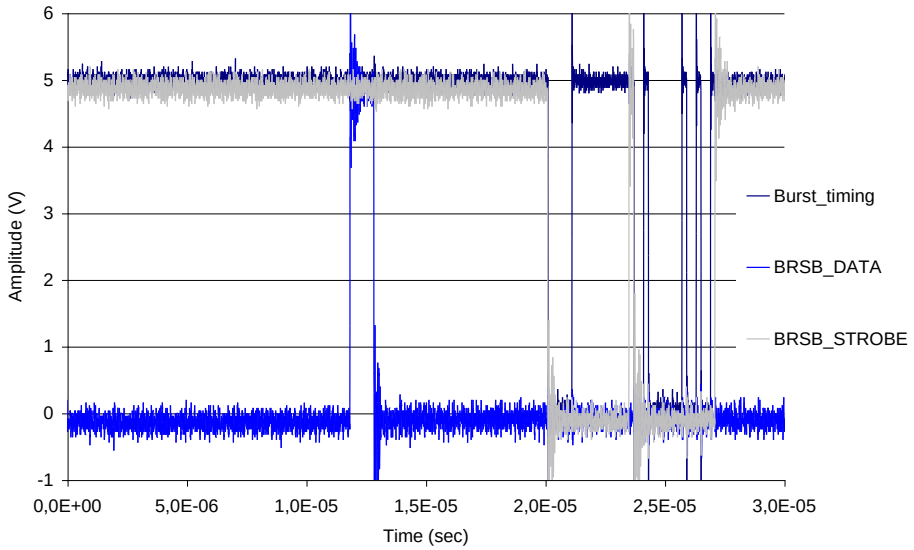

Figure 5.7-1: BURST_TIMING signal (IC50-7)
BRSB_DATA_DOWN signal (IC50-15)
BRSB_STROBE_DOWN signal (IC51-1).

5.8 BURST FIFO MANAGEMENT

When used with the SEM-MCAL TE, if the TE FIFO is half full, the BRSB_BUSY_UP signal is sent to the SEM electronics, that suspends the transmission of data to TE.
If an event is being sent when the busy signal arrives, the data of that event is sent, but any further data is sent to the TE. As soon as the TE stops sending the BRSB_BUSY_UP, data transmission from the SEM is recovered (see Figure 5.8-1).
The recovering of data generation and SEM-MCAL's FIFO filling occurs immediately whatever is number of data still inside the SEM-MCAL's FIFO.
So if the rate of data generation is sustained, it may happen that the SEM-MCAL's FIFO works near its level of maximum filling. The effect is that the rate of data processed diminish probably due to the time loss in the management of the SEM-MCAL's FIFO full situation (see Figure 5.8-2).
A reset of SEM-MCAL's FIFO restore the full functionality of the system. The same can be probably obtained with a different management of the FIFO that completely empties it before restoring data acquisition.

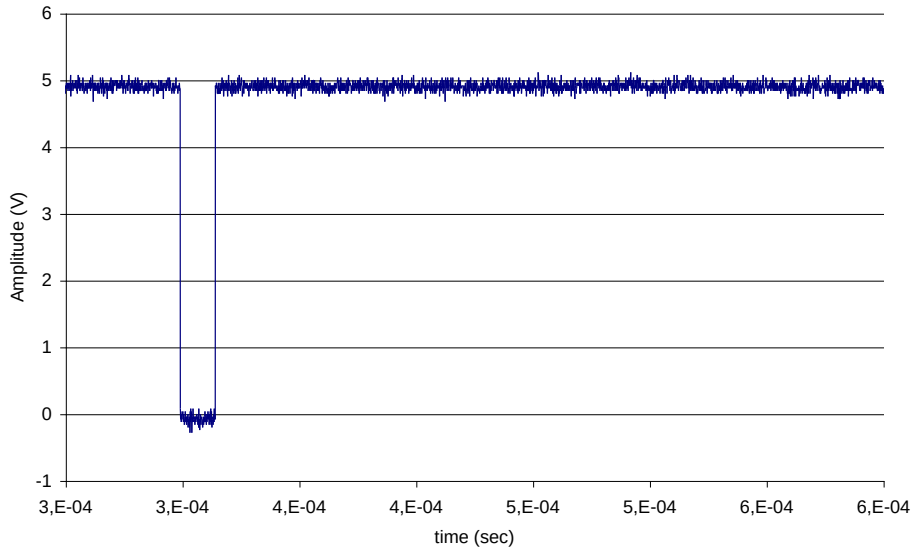

Figure 5.8-1 Burst FIFO Half-full becomes true (low) when the data are not received from the TE, if the transmission is recovered the FIFO works again.

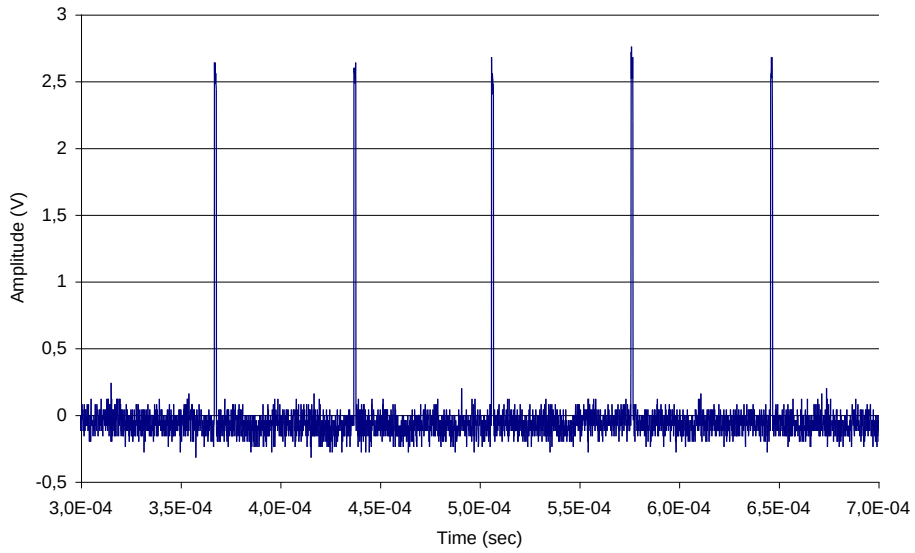

Figure 5.8-2 Burst FIFO Half-full (true low) for high count rates. The FIFO is almost always busy.

5.9 GRID ANALOGUE CHAIN

The analogue chain of the GRID chain is in common with the Burst chain up to the stretcher circuit. The stretching of the analogue signals is commanded by an external T1_YES signal that is delayed to generate the GRID_HOLD signal.
All the bars events has then converted and transmitted.
Figure 5.9-1 shows the relation between the signals of the GRID chain
In Figure 5.9-2 the main ADC signals are shown; both sides of all the 30 bars are converted. The ADC clock generates one period for every signal to be converted plus two periods (62 clock period total).
GRID data are then formatted stored in GRID FIFO and transmitted via the GSB bus as described in Figure 5.9-3
If data cannot be received, the GSB_BUSY_UP signal has to be sent to the SEM electronics.
This suspends the transmission of data to TE. If an event is being sent when the busy signal arrives, all the data of that event is sent.
As soon as the BRSB_BUSY_UP is not true, data transmission from the SEM is recovered.

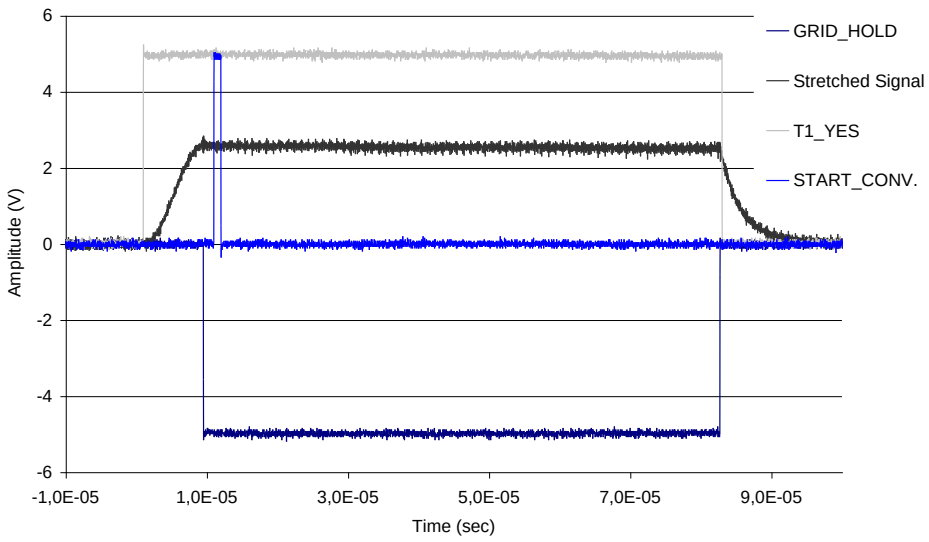

Figure 5.9-1 Relation between the signals of channel 5A stretcher.

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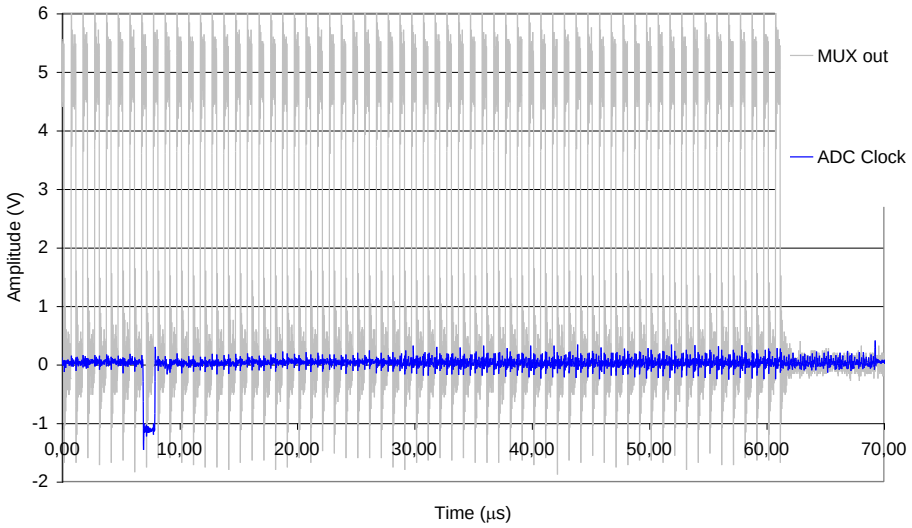


Figure 5.9-2 GRID ADC signals , ADC input and ADC clock. Just ch 5A has been stimulated

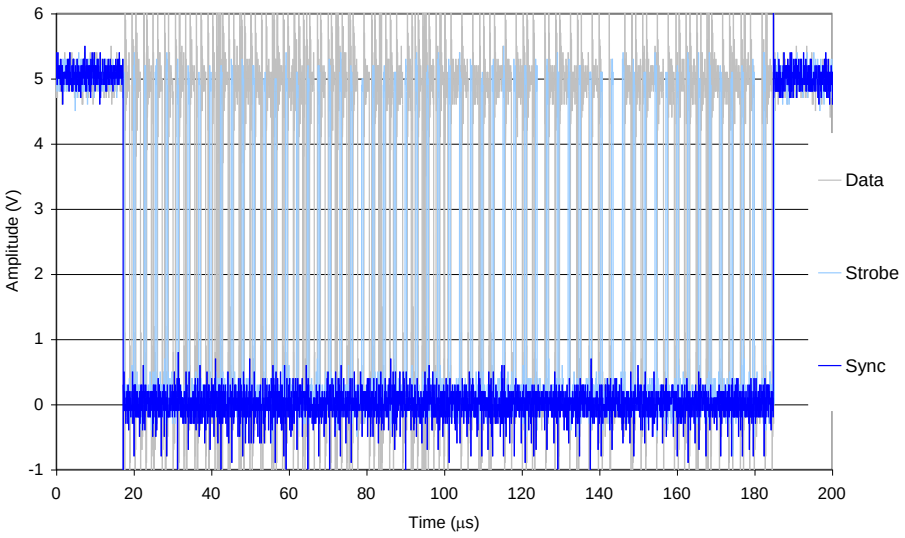


Figure 5.9-3 Signals sent from SEM electronics to SEM TE. Signals have been probed in TTL format prior conversion to LVDS

5.10 HOUSEKEEPING AND TELECOMMAND

It has been verified the correct receiving and implementation of the telecommands (Table 3.3-1) configuring the system.

It has been verified that the rate-meters HK are implemented in SEM.
The HK ratemeter information is sent out every 16 sec.
Two rate-meter route on all the discriminator of BoardX and of BoardZ respectively. Each ratemeter is then refreshed every 45x16 sec.
Two rate-meter on the two board are continuously refreshed with the contain of two discriminators selected via TC.

The rate-meters have not been calibrated.

6. MCAL SEM PERFORMANCE TESTS

6.1 PERFORMANCE TEST FLUX

In the following are reported details of the SEM performances tested. The test were done with the aim of verifying the fulfillment of SEM-MCAL requirement .
The flux of the SEM-MCAL test is depicted in Figure 6.1-1

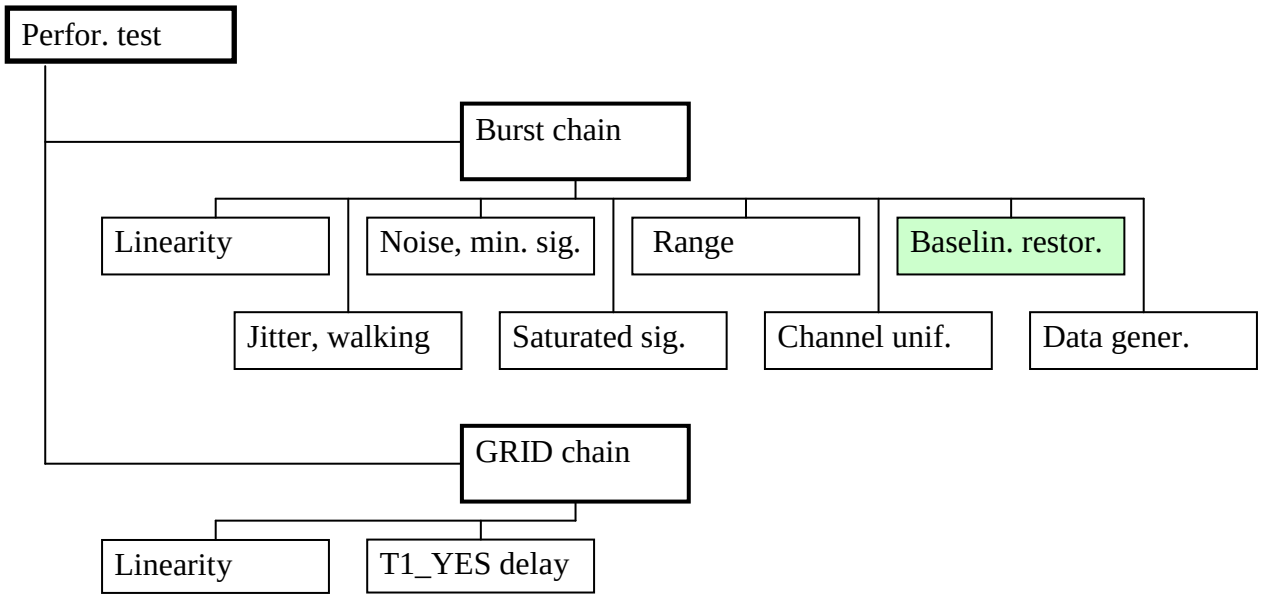


Figure 6.1-1 Functional test flux: green box indicate good behaviour.

6.2 LINEARITY OF THE BURST CHAIN

Ch 23A has been measured for linearity using both Burst and GRID data.
Different charge levels are generated by a pulser and injected into the pre-amplifier with a calibrated capacitor.
The pre-amplifier is (see document RD [3]) was connected to 2 photodiodes for a total area of 2 cm^2. The sensitivity of the pre-amplifier is about 3.66 $\mu V/e^-$.
The output of the preamplifier is connected to the SEM-MCAL via a buffer amplifier with a gain of about 5. This buffer amplifier has been added to have a greater detail of the peaks and has to be taken into account when considering the operative range of the system.

Data are collected with the SEM-TE and the spectra of Burst and GRID are then reconstructed.
For each charge level the centroid of the peak is evaluated.
The result for the Burst chain is resumed in Table 6.2-1 and in Figure 6.2-1 and Figure 6.2-2.
Due to the buffer on the pre-amplifier the maximum signal of Table 3.6-1 correspond to about 250 MeV. The linearity exceed the +/- 1% required.

Pulser Signal amplitude (V)	Charge (e^-)	Energy * (MeV)	Ch	Peak FWHM ch
0.02	15300	1.0	188	13.3
0.05	38100	2.5	310	12.1
0.1	76300	5.1	519	11.5
0.15	114400	7.6	715	12.2
0.2	152600	10.2	919	12.0
0.3	228800	15.3	1318	12.0
0.4	305100	20.3	1712	11.8
0.5	381400	25.4	2101	11.7
0.6	457700	30.5	2484	12.3
0.7	534000	35.6	2865	12.2
0.8	610200	40.7	3236	12.3
0.9	686500	45.8	3603	12.2
1.0	762800	50.9	3963	12.2

Table 6.2-1 Channel peak of the Burst chain for different pulse amplitudes.
NB: there is a buffer with gain 5 between the pre-amp and SEM.
*** Energy evaluated at 1 cm from the PD considering a light output of 15 e/keV**

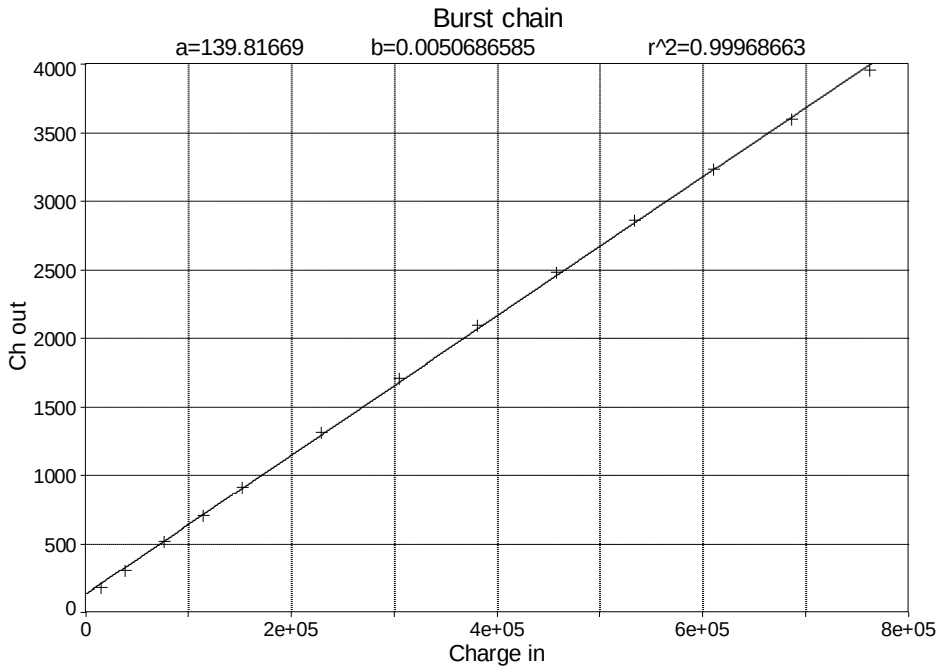


Figure 6.2-1 Position of the peaks in ADC channel for the Burst chain

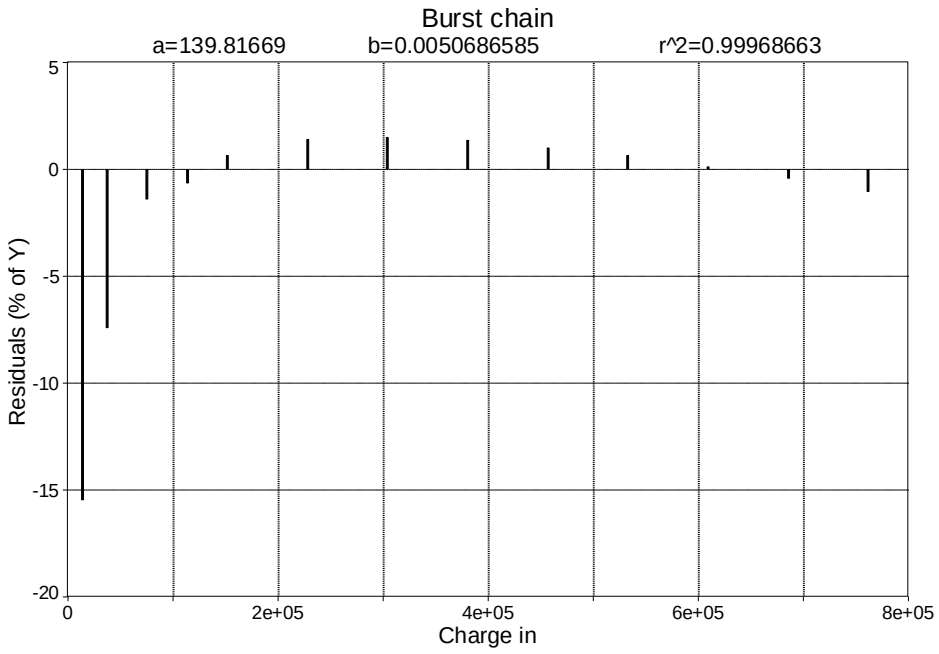


Figure 6.2-2 Residual (in %) of the peaks position for a linear fit

6.3 BURST CHAIN NOISE EVALUATION.

Using the data of paragraph 6.2 the noise of one channel can be evaluated from the width of the measured peaks.
The noise is mainly due to pre-amplifier and PD and should not be increased by the amplifying stages of SEM MCAL.

For the burst chain the width of the peaks measured in 6.2 is about 12.3 ch.
Using the parameters of Figure 6.2-1 this correspond to a noise level of about 1000 e^- rms.
On RD [3] the noise measured was betweeen 925 and 1100 e- rms depending on the shaping time of the amplifier.
It can be concluded that SEM-MCAL does not introduces further noise.

6.4 BURST CHAIN MINIMUM DETECTABLE SIGNAL

In the Burst chain, using the assumptions of Table 6.2-1 the minimum detectable signal at about 1 cm from the PD due to noise limitation is about 5000 e- i.e. a 330 keV deposit.
In the measures reported in paragraph 6.2 the pre-amplifier is connect to the SEM MCAL with a buffer amplifier with a gain of about 5.
The buffer amplifier has the effect of increasing the signal and the noise of the pre-amplifier of the same rate so that the above consideration are still valid.
Therefore the effect described in 5.4 put a limitation on the minimum value in the setting voltage of the threshold.
Independently of the noise level the threshold must be placed below 590 mV (see Figure 5.4-4) i.e. at least 220 mV from the BLR output level.
From a quick calibration of ch 5A reported in Table 6.4-1 it result that the minimum charge is about 29650 e^-; notice that the data reported in Table 6.4-1 are obtained with a buffer amplifier with gain 5 between the pre-amp and SEM-MCAL.

Thr setting on TE	Ref Voltage (mV)	Ch min.	Eq. Charge e^-
180	550	295	30600
200	610	288	29200
220	670	280	27650

Table 6.4-1 Correspondnce for the voltage setting and the minimum channel counting. The relation between minimum charge detectable (in ke^-) and thr (in mV) is min_ch = 44150 - 24.583*thr

6.5 RANGE EVALUATION OF THE BURST CHAIN

Using the noise value determined in paragraph 6.3 it result that the minimum charge and energy that is well above the noise are
Charge min 5000 e^- Energy min @ 1cm from PD ~ 350 keV
Where the assumption of a light output of 15 e^-/keV in the bar detector is done.

BUT

Considering the effect described in 6.4, the threshold cannot be placed below a minimum voltage value of about 550 mV i.e. , considering also the gain of the buffer amplifier used in these measure between the pre-amp and sSEM-MCAL the minimum detectable energy at 1 cm is about 10 MeV.

Using the data shown in paragraph 6.2 and considering that during the measures a buffer amplifier with gain 5 was used the maxim charge and signal detectable are

Charge max 3.8 x 10^6 e^- Energy max @ 1cm from PD 250 MeV

6.6 BURST CHAIN BASELINE RESTORER (BLR) EVALUATION

Scope of the test is to evaluate the effect of the Baseline Restorer circuit.
The input of the analogue chain 5A was stimulated with a pulser generating random pulses with different averages frequences.
The baseline level of the shaper output (IC U202A pin 1) and of the baseline restorer output (IC U202A pin 7) were measured

The baseline of the shaper output was found sensitive to pulse frequencies greater than 250 Hz.

The baseline of the BLR output (about 850 mV) does not changes for pulses rates up to 25 kHz.

6.7 BURST CHAIN DISCRIMINATOR: JITTER AND WALKING TIME

As described in the paragraphs 5.5 and 5.7 the BURST TIMING signal should be used in DH or TE to time mark an event.
To evaluate the jitter and walking time of this signal it was measured the delay between the signal stimulating in input of the bar 5 chain and the hold command (related to BURST TIMING) produced on that chain.
An oscilloscope was triggered by the pulse generator injecting the charge in the channel under test and the delay between trigger and Hold signal, averaging the signals of the last 128 waveforms was read.
Result are resumed in Table 6.7-1

Pulser Signal amplitude (V)	Charge (e^-)	Energy * (MeV)	Delay from trigger (μs)	Jitter (μs)
Ch 5 side A				
0.02	15300	1.0	9.65	~ 2.0
0.2	152600	10.2	9.38	~ 0.2
0.6	457700	30.5	9.14	~ 0.1
0.8	610200	40.7	9.12	~ 0.1
1.0	762800	50.9	9.12	~ 0.1
Ch 5 side B				
0.02	15300	1.0	~9.6	~ 2.0
0.2	152600	10.2	9.40	~ 0.2
0.6	457700	30.5	9.24	~ 0.1
0.8	610200	40.7	9.22	~ 0.1
1.0	762800	50.9	9.22	~ 0.1
Ch 5 Sum				
0.02	15300	1.0	~10.0	~ 2.0
0.2	152600	10.2	9.56	~ 0.2
0.6	457700	30.5	9.30	~ 0.1
0.8	610200	40.7	9.27	~ 0.1
1.0	762800	50.9	9.26	~ 0.1

Table 6.7-1 Delay between a stimulated pulse and BURST_HOLD for bar 5 and jitter of BURST_HOLD.
*** Energy evaluated at 1 cm from the PD considering a light output of 15 e/keV**

There is no significatife difference betweent the timing of the three discriminator of one bar.
The maximum walking time is about 0.75 μs while the maximum jitter is about 2.0 μs

6.8 CONTINUITY OF BURST DATA ACQUISITION

SEM-MCAL was tested on the field connecting to it 8 bars detectors with pre-amplifier and with gamma rays and particles produced at CERN. The buffer with gain 5 between pre-amp and SEM MCAL was present for all the bars but #23.
The spill of particle was hitting the detector every few second.
The time profile of the rate of data collected in one bar is depicted in Figure 6.8-1.
Gaps can be seen on the stream of data due to a blocking of the SEM_MCAL.
To recover from this blocking a periodic Burst_FIFO reset TC was sent.
The effect is a confirmation of the behavior described in 5.4 and 5.8.

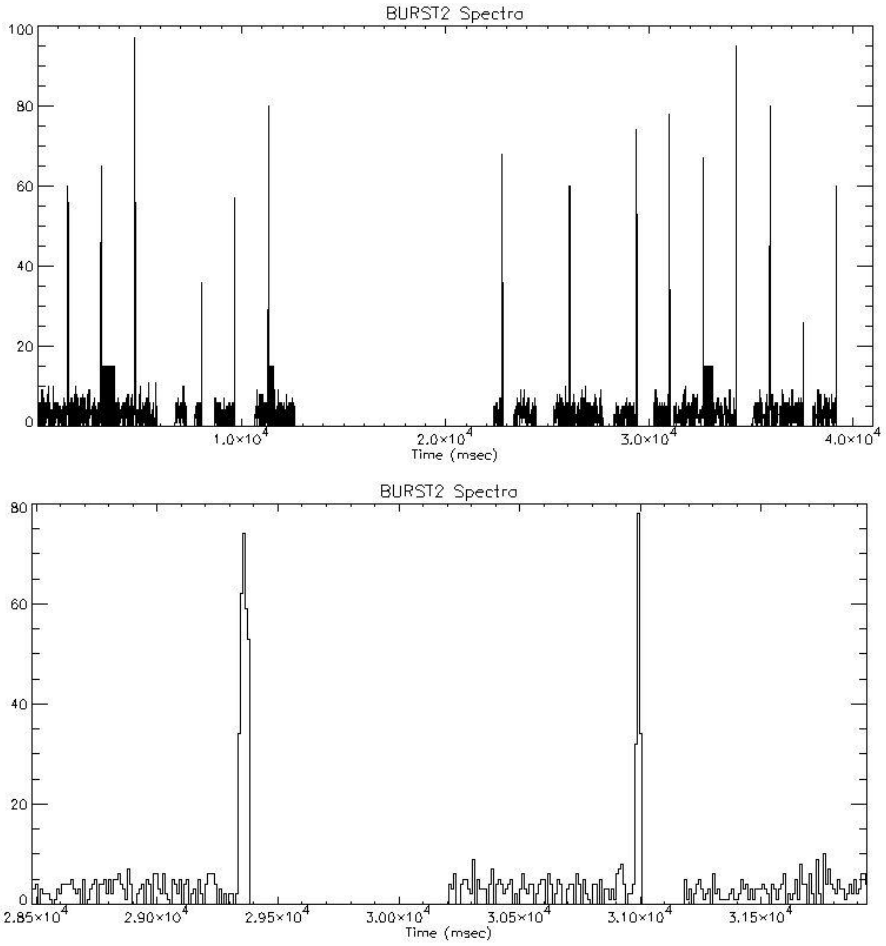


Figure 6.8-1 Rate of data collected on bar 7 during the test at CERN on August 2003 (bottom: zoom of the top image). On X axis there is a factor of scale in the timing. To have the correct timing a factor 50x should be used. On y axis are reported the counts integrated in the time bin.

6.9 BURST CHAIN: UNIFORMITY OF THE CHANNELS

Scope of this test is to verify that all the channels in the Burst chain are analysed with the same priority.
SEM-MCAL was tested connecting to it 8 bars detectors with pre-amplifier and collecting a background spectra with all the threshold (but bar 23) at the same value (see Figure 6.9-1).
In Figure 6.9-2 the rate of collected data in the same period for all the bar is shown.
It result a different sensitivity, that can be partially accounted to the sensitivity of the bar detector itself, but also a great inefficiency of the channels of the BoardZ and many dead periods for all the bars with the exception of bar 4.

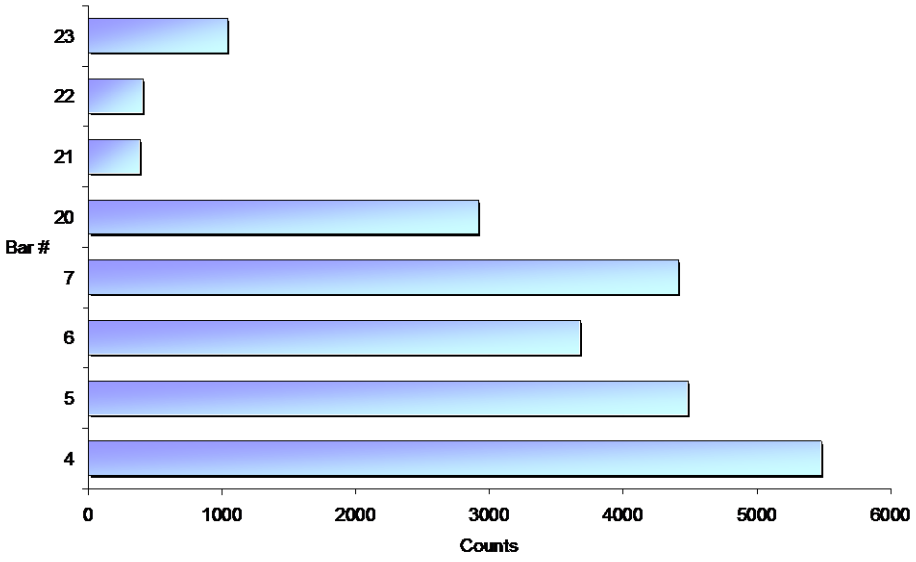
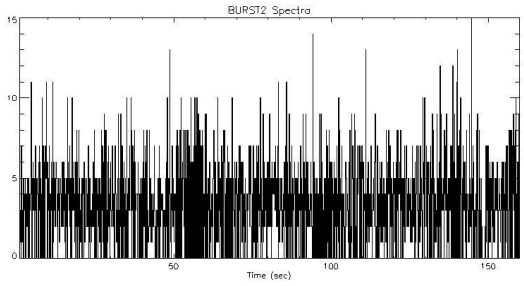
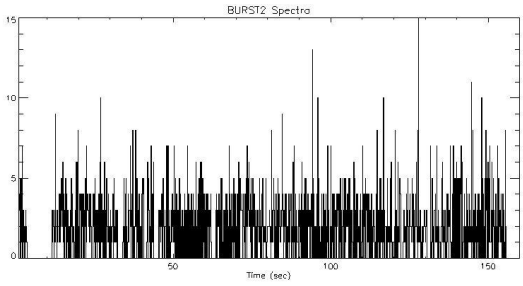


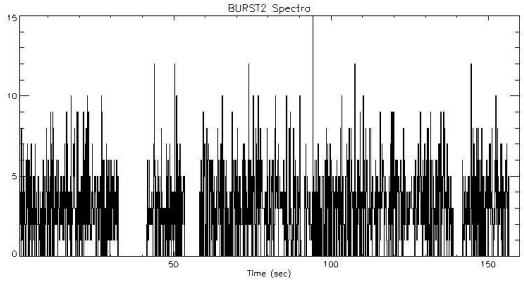
Figure 6.9-1 Counts distribution on the different bars for 160 sec background. All the bars, but #23, have the same threshold.



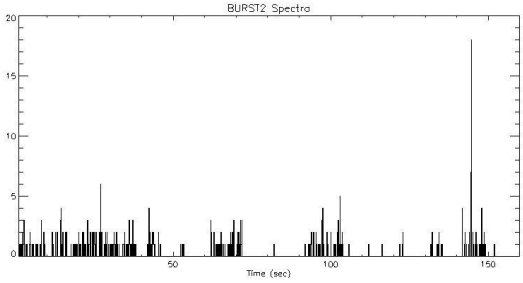
Bar 4 (y_axis range: 0 ÷ 15)



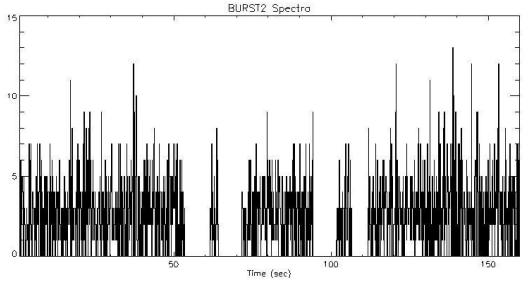
Bar 20 (y_axis range: 0 ÷ 15)



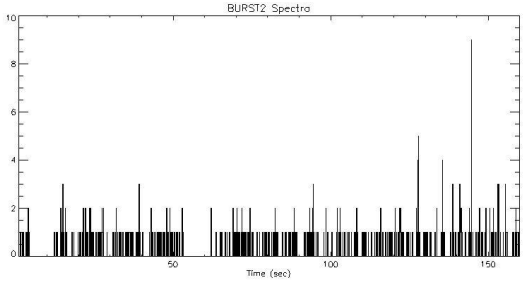
Bar 5 (y_axis range: 0 ÷ 15)



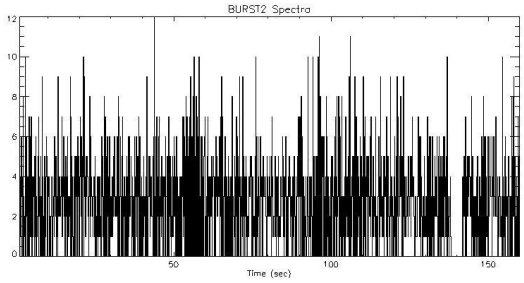
Bar 21 (y_axis range: 0 ÷ 15)



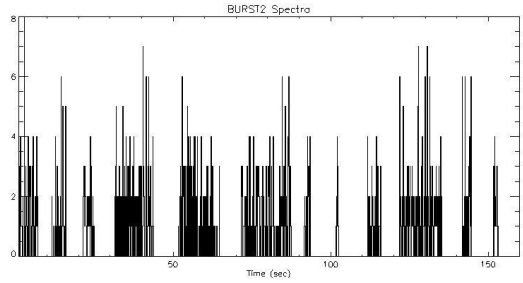
Bar 6 (y_axis range: 0 ÷ 15)



Bar 22 (y_axis range: 0 ÷ 10)



Bar 7 (y_axis range: 0 ÷ 12)



Bar 4 (y_axis range: 0 ÷ 8)

Figure 6.9-2 Background count of the various bar The x_ axis range is 0 ÷ 160 sec for all the plots

6.10 LINEARITY OF THE GRID CHAIN

Following the same procedure of paragraph 6.2 ch 22A has been used to test the GRID chain
The result for the Burst chain is resumed in Table 6.10-1and in and Figure 6.10-1 and Figure 3.6-3.
The ADC range is limited to 2048, instead of the 4096 foreseen, due to the fact that the double gain has not been implemented.
Due to the buffer on the pre-amplifier the maximum signal of Table 6.10-1 correspond to about 1 GeV .
The linearity exceed the +/- 1% required.

Pulser Signal amplitude (V)	Charge (e^-)	Energy * (MeV)	Ch	Peak FWHM ch
0.05	38150	2.55	93	3.4
0.1	76300	5.1	149	5.8
0.15	114400	7.65	205	5.7
0.2	152550	10.15	261	6.2
0.4	305100	20.35	484	See par. 6.11
0.6	457650	30.5	704	“
0.8	610250	40.7	921	“
1	762800	50.85	1131	“
1.2	915350	61	1335	“
1.4	1067900	71.2	1527	“
1.6	1220450	81.35	1700	“
1.8	1373000	91.55	1845	4.1

Table 6.10-1 Channel peak of the GRID chain for different pulse amplitudes.
NB: there is a buffer with gain 5 between the pre-amp and SEM.
*** Energy evaluated at 1 cm from the PD considering a light output of 15 e/keV**

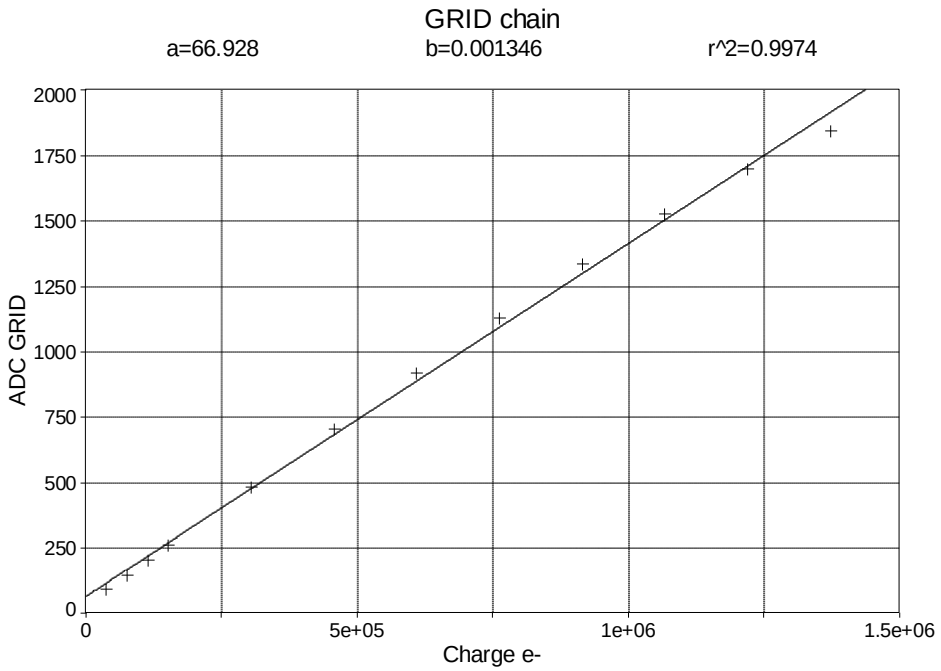


Figure 6.10-1 Position of the peaks in ADC channel for the GRID chain

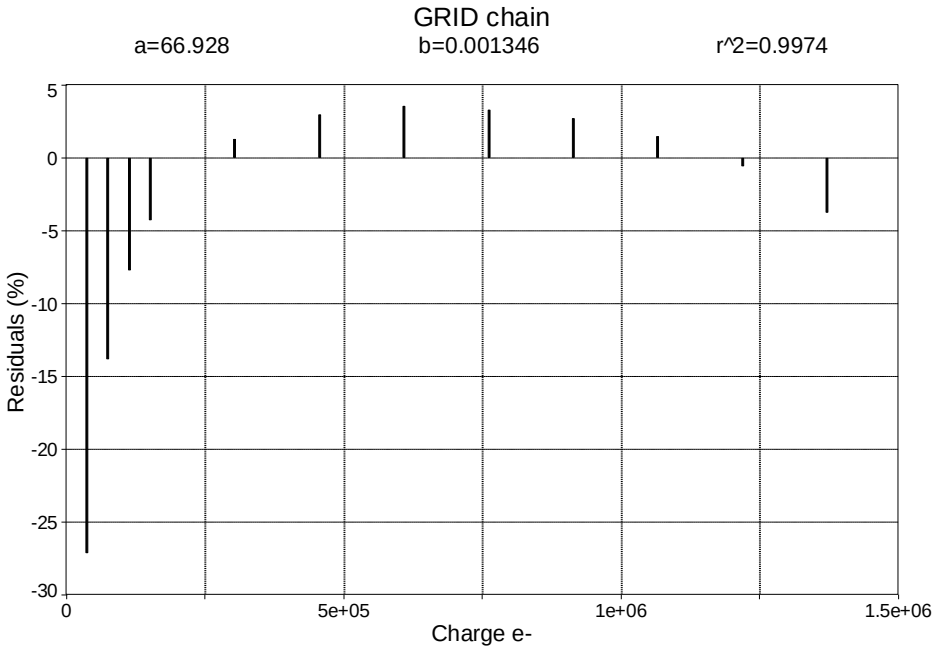


Figure 6.10-2 Residual (in %) of the peaks position for a linear fit

6.11 GRID CHAIN NOISE EVALUATION

With the same technique used in paragraph 6.3 and the data of paragraph 6.2 the noise of one channel can be evaluated from the width of the measured peaks.
However, the width of the peaks measured in the GRID chain depends strongly from the correct setting of delay between the T1_YES and GRID_Hold signal (see paragraph 5.9).
As it can be noticed in Figure 6.1-1 maintaining constant this delay, the peaks in the central part of the spectra are wider than the other ones.

For the GRID chain evaluation considering the narrowest peak of paragraph 6.2 (3.4 ch) the noise result 1070 e^- rms.

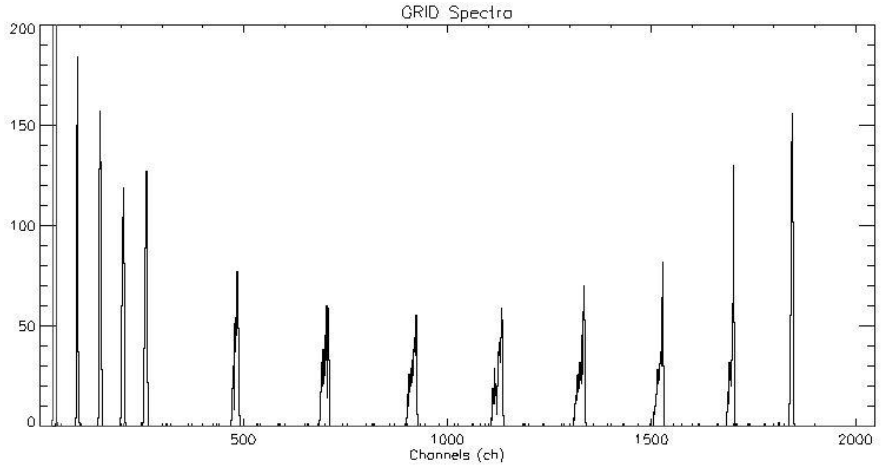


Figure 6.11-1 GRID spectra: peaks induced in ch 22A to test the linearity of the system. The peaks are generated with a pulser that is also used to generate the T1_YES signal. The delay between T1_YES and GRID hold has been maintained constant.

6.12 DELAY BETWEEN T1_YES AND GRID_HOLD

The shape of the peaks in Figure 6.11-1 shows that there is a dependence of the peaks width from the delay between T1_YES and GRID_HOLD.
Further measures on ch 22A where this delay is changed are reported in
Table 6.12-1
The increase in the delay does not improve the performances.

Pulser Signal amplitude (V)	Charge (e^-)	Ch peak	Peak FWHM ch
Delay 43h in TE			
0.1	76300	152	2.8
1.0	763000	1133*	3.5
2.0	1525600	1936	61
Delay 48h in TE			
0.1	76300	150	4.2
1.0	763000	1131*	8.4
2.0	1525600	1961**	8.2

Table 6.12-1 Peak position and width for different delay between T1_YES and GRID_HOLD signal
***The peak show a tail on the lower energy side of about 15 ch**
**** The peak is very irregular**

6.13 RANGE OF THE GRID CHAIN

Using the noise value determined in paragraph 6.11 it result that the minimum charge and energy that is well above the noise are

Charge min 5500 e^- Energy min @ 1cm from PD 370 keV

Where the assumption of a light output of 15 e^-/keV in the bar detector is done.

Using the data shown in paragraph 6.2 and considering that during the measures a buffer amplifier with gain 5 was used the maxim charge and signal detectable are

Charge max 6.85 x 10^6 e^- Energy max @ 1cm from PD 450 MeV

APPENDIX A: MCAL ELECTRICAL INTERFACE.

MCAL Subsystem exchange signals with PDHU through two connectors:
GRID connector (Table A1)
Burst Connector (Table A2)
Each calorimeter board will be powered-up through a 9pinconnector (Table A3):

Pin N°	Name	Type	Levels	In/Out (PDHU	Active ...	Description
15	GSB_BUSY_UP_P~	D	LVDS	O	L	Grid Serial Bus: Ative Low Halt for 64 serial energy transfer from PDHU
2	GSB_BUSY_UP_M~	D	LVDS	O		
13	GSB_DATA_DWN_P	D	LVDS	I	-	Grid Serial Bus: Data Line
25	GSB_DATA_DWN_M	D	LVDS	I	-	
12	GSB_STROBE_DWN_P~	D	LVDS	I	L	Grid Serial Bus: Active Low STROBE
24	GSB_STROBE_DWN_N~	D	LVDS	I		
11	GSB_SYNCH_DWN_P~	D	LVDS	I	L	Grid Serial Bus: SYNCH for 64 serial energy. Active Low
23	GSB_SYNCH_DWN_N~	D	LVDS	I		
14	MCAL_HK_CK_P	D	LVDS	O	-	CK to increment AnHK MUX
1	MCAL_HK_CK_M	D	LVDS	O	-	
21	MCAL_Y_ANHK	Analog	0..2.5V		-	Mux-ed analog line
8	MCAL_Y_ANHK_RET	Analog	N.A.		-	
16	START_CONVERSION_P	D	LVDS	O	H	After "positive" 1.5 Level trigger (GRID); Pulse 200n
3	START_CONVERSION_M	D	LVDS	O		
17	T1_YES_P	D	LVDS	O	H	(for HOLD and Reset); State
4	T1_YES_M	D	LVDS	O		
20	MCAL_SURV_MON	Analog	TBD		-	No processing
7	MCAL_SURV_MON_RET	Analog	TBD		-	
5	Spare					
6	Spare					
9	Spare					
10	Spare					
18	Spare					
19	Spare					
22	Spare					

Pin Avail: 25
Pin Used: 18
Pin Spare: 28%

Table A1 GRID connector: _UP means "to MCAL FrontEnd" and _DWN "to PDHU".

Pin N°	Name	Type	Levels	In/Out (PDHU	Active ...	Description
12	MCAL_AC_P	D	LVDS	O	H	Logic Network on AC_DFE Board in PDHU Box.
30	MCAL_AC_M	D	LVDS	O		
19	BRSB_BUSY_UP_P~	D	LVDS	O	L	Burst Serial Bus: Active Low Halt for serial transfer from PDHU
37	BRSB_BUSY_UP_M~	D	LVDS	O		
11	BRSB_DATA_DWN_P	D	LVDS	I	-	Burst Serial Bus: Data Line
29	BRSB_DATA_DWN_M	D	LVDS	I	-	
10	BRSB_STROBE_DWN_P~	D	LVDS	I	L	Burst Serial Bus: Active Low STROBE
28	BRSB_STROBE_DWN_M~	D	LVDS	I		
9	MCAL_BSB_DATA_DWN_P	D	LVDS	I	-	Bidirectional Serial Bus: Configuration Data Line (from PDHU)
27	MCAL_BSB_DATA_DWN_M	D	LVDS	I	-	
15	MCAL_BSB_DATA_UP_P	D	LVDS	O	-	Bidirectional Serial Bus: Digital HK Data Line (to PDHU)
33	MCAL_BSB_DATA_UP_M	D	LVDS	O	-	
8	MCAL_BSB_STROBE_DWN_P~	D	LVDS	I	L	Bidirectional Serial Bus: Active Low STROBE Line to PDHU
26	MCAL_BSB_STROBE_DWN_M~	D	LVDS	I		
14	MCAL_BSB_STROBE_UP_P~	D	LVDS	O	L	Bidirectional Serial Bus: Active Low STROBE Line From PDHU
32	MCAL_BSB_STROBE_UP_M~	D	LVDS	O		
21	BURST_TIMING_P	D	LVDS	I	H	Timing Line for Burst Event W=1us sinch with CK1 rising edge (re-routed to SAIE as MCAL-AC sig.)
2	BURST_TIMING_M	D	LVDS	I		
20	MCAL_CK5_DWN_P	D	LVDS	I	-	5 MHz CLOCK to PDHU
1	MCAL_CK5_DWN_M	D	LVDS	I	-	
17	MCAL_CK5_UP_P	D	LVDS	O	-	5 MHz CLOCK from PDHU
35	MCAL_CK5_UP_M	D	LVDS	O	-	
18	MCAL_CL_FIFO_P~	D	LVDS	O	L	Active Low Clear FIFO (for synch. purposes); 200ns
36	MCAL_CL_FIFO_M~	D	LVDS	O		
22	MCAL_HTHR_P	D	LVDS	I	H	Pulse 1us; FAST TRIGGER (HighThreshold)
3	MCAL_HTHR_M	D	LVDS	I		
16	MCAL_RESET_P	D	LVDS	O	L	to RESET the BOARD. Pulse min 200ns
34	MCAL_RESET_M	D	LVDS	O		
13	SYNCH16_P	D	LVDS	O	H	Synch. signal for dig. HK update;Pulse 1us, period 16sec; synchr. with rising edge CK5
31	SYNCH16_M	D	LVDS	O		
25	MCAL_X_ANHK	Analog	0..2.5V	O	-	Mux-ed analog line
6	MCAL_X_ANHK_RET	Analog	N.A.	O	-	
4	Spare					
5	Spare					
7	Spare					
23	Spare					
24	Spare					

Pin Avail: 37
Pin Used: 32
Pin Spare: 14%

Table A2 Burst connector: _UP means "to MCAL FrontEnd" and _DWN "to PDHU".

Pin	Name	Type	Ratings	Description
1	MCAL_+5V_DIG	Power	5V/0.6A	+5V Digital Supply Voltage for MCAL
6	MCAL_+5V_DIG_RTN	Power	0V/0.6A	
5	MCAL_-28V_BIAS	Power	28V/5mA	-28V Bias Voltage for MCAL
4	MCAL_-28V_BIAS_RTN	Power	0V/5mA	
2	MCAL_+5V_AN	Power	5V/0.5A	± 5V Analog Supply Voltage for MCAL
7	MCAL_-5V_AN	Power	5V/0.5A	
3	MCAL_± 5V_AN_RTN	Power	0V/0.5A	
8	Chassis	GND	0V/0A	Cable Shield Connection
9	Spare			

Table A3 Power supply connector

APPENDIX B: SEM-MCAL TEST EQUIPMENT COMMANDS

On Host Computer: HK monitoring
Switch on the Host Computer (SC4)
Username: agifee
Password: TESREfee

To start the HK monitoring SW:
Command: testmcal & --- Goes in the program directory and runs it.
In testmcal:
Menu hkconf
In hkconf:
hk pulse enable --- Starts the SYNCH_16 signal, afterwards hkconf can be closed.

Command: mmcconsole & --- Runs the main program.
In mmcconsole:
Menu Status --- Monitoring of the ratemeters from board X and board Z.

On Host Computer: manual BURST acquisition without saving data
Command: mmcconsole & --- Runs the main program.
In mmcconsole:
Menu Acquisition -> DFE configuration
General -> Global Reset Button
Set DAC_REF to 118: write --- This command sets the threshold of all the reference DAC to about 600mV, afterwards every DAC can be set individually with respect to this one.
Set the values of the single thresholds in DACX for the X board, and in DACZ for the Z board. Valid numbers are between 0 and 255 (255 = DAC_REF, 0 = 0V).
Set Time Delta Register to 31 --- This register defines the time between the T1_START and the START_CONV signals. Used only in GRID mode.
Idle\Observation Button --- When in Observation mode the data acquisition is started, in Idle the acquisition is stopped.
Menu Acquisition -> Acquisition -> Start Burst Acquisition --- The TE starts to download data from the SEM FIFO. Some times it may be necessary to reset the FIFOs to restore the acquisition

On Host Computer: GRID acquisition without saving data
Command: testmcal &
In testmcal:
Menu GRID -> GRID: Read memory
Select: *Output* and *Ext T1 start*
Output --- The output data from SEM electronics to TE is displayed on screen. The data displayed is in 11 bit format (12 bits displayed, of the which the first is always 0).

Ext T1 start --- In this mode the data acquisition is started by the external T1_YES signal, otherwise will be started internally.

Start Test button --- Pressing this button will start the reading of GRID events, the system will wait for an incoming event. When an event arrives data is displayed on screen (if the output option is selected).

N.B. The data displayed is in 11 bit format, going from 000 0000 0000 of the lowest possible value (0V) to 111 1111 1111 (+2.5V). As the ADC is used in –2.5 – +2.5 V mode, when a negative reading is performed the resulting value ranges from 000 0000 0000 (-2.5V) to 111 1111 1111 (0V). This can cause misunderstandings between saturated events and noise events, both readings would be close to 111 1111 1111.

On Host Computer: Reset TE FIFO and SEM FIFO

Command: testmcal &
In testmcal:

VME -> VME: Read and write memory

Double click on BURST --- The address of the BURST board is displayed on the upper side of the window.

Upper right side of the window, box named WRITE: set Address=0x08 and Data=0x03.

Button WRITE --- The TE sends the command BRSB_CL_FIFO_UP to the SEM in order to reset the SEM FIFO and the TE FIFO.

Access to Science Consolle SC3 from Host computer

ssh –l agile agilesc3
Password: SC3ast03

On Science Consolle Acquire and save data

Command: cpanel &
In configure acquisition press OK
In Acquisition (3) start acquisition
To stop: press Clean then Quit

On Host Computer start acquisition to save data on Science Consolle

Command: mmcconsole & --- Runs the main program.
In mmcconsole:
Menu Acquisition
(if needed ch'ange the IP address of Science Consolle 192.167.166.89)
Start Burst acquistion (to acquire from Burst)

Start GRID acquisition (to acquire from GRID)
Start HK acquisition (to acquire fromHK)
Start sender (to allow connection with Science Consolle)
OR Start all
Connect (to send data to Science Consolle)
Start (to start the measure with relative run id)
Stop (to stop the measure)
Disconnect (to disconnect from Science Consolle)

On Science Consolle run program display and analysis data

ssh –l agile agilesc3
Password: SC3ast03
idlde (run IDL)
open project /home/agile/Celesti/Analisi_Dati_SEM/…prj (run program)
data in /data1/archive/erdf/…..