CZT Bo/Pa Set-up
for the hybrid experiment at the Leicester University

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Aims

This document intends to provide the user with the technical informations to reliably arrange and manage the set-up of the CCD detector (Leicester) and the CZT detector (Bologna-Palermo). **The documentation mainly refers to the CZT detector equipments.**

1. Documents Applicable

CZT	*Characterization of a CZT Focal Plane Small Prototype for Hard X-Ray Telescope*	IEEE 2004
CCD	*Developments in MOS CCDs for X-ray astronomy*	NIM A 436 1999
	Spectral re-distribution and surface loss effects in Swift XRT (XMM-Newton EPIC) MOS CCDs	NIM A 484 2002
ASIC	*Low power BiCMOS ASIC for wide energy range X-gamma ray imaging and spectroscopic detectors*	NIM 2004
Read-Out	*Simulatore hardware e elettronica di back up*	PLX-IASF-001
SW	*Quick-look SW manual*	PLX-IASF-003

2. Summary

The scientific objectives of next high throughput mission in X-ray astronomy require new type of focussing telescopes able to extend the observational range at least up to 100 keV to solve crucial question concerning the nature of the high energy emission from cosmic source and the origin of the cosmic X-ray background. A challenging technology to extend the classical grazing incidence range to higher energy is today offered by the development of multilayer optics that are effective as X-ray concentrators between few keV up to 80/100 keV. A useful arrangement for this type of mission concept (e.g. HEXIT, SIMBOL-X) can foresee the soft (e.g. 0.1-10 keV) X-ray optics nested and coaxial with the hard-X mirrors. This means that the focal plane of the telescope shall operate on the overall energy range (from 0.1 to 80/100 keV) fulfilling at the best the different requirements of the two optics type in terms of detection efficiency, spatial resolution and spectroscopic performance. A solution for this kind of focal plane detector is given by an hybrid design with a soft X ray detector (e.g. CCD) in front and coaxial to an hard-X ray detector (e.g. Pixel CZT spectrometer).
In this contest our collaboration (Space Research Centre of the Leicester University and INAF/IASF-Bologna/Palermo) had the idea to assemble a hybrid detector prototype using as soft X-ray detector a spare CMOS CDD of the EPIC/XMM developed at Leicester University instrument and a CZT small pixel detector, available at IASF/INAF, with custom ASIC's (developed in collaboration with Politecnico of Milano) as analogic front-end electronics. The main characteristics of the two detectors are shown in Table 1.
This report is divided in two main parts: the first contain documentations about the electronics, designs, cabling schemes and electrical interfaces for the CZT pixel detector and is intended as a reference manual for the experimental set-up of the hard X-ray detector at Leicester University, the second is mainly a log-book of the first phase activities yield at the same place during the week (25-29 July 2005) devoted to the hybrid detector set-up and functional test.

Detector	Type	Operative Range	Spatial resolution	Energy Resolution	Efficiecy
CZT	Pixellated CdZnTe	10-100 keV	500 μm	~ 5% @ 60 keV ^{241}Am	~90% @ 60keV
EPIC CCD22	MOS CCD	0.2 -10 keV	40 μm	~ 3% @ 3 keV ~ 2% @ 10 keV	~ 80% @ 3 keV ~ 25% @10 keV

Table 1. The main characteristics of the two detectors used for the Hybrid prototype.

3. The CZT ASIC

Annex 1

Low power BiCMOS ASIC for wide energy range X-gamma ray imaging and spectroscopic detectors

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Abstract

A low-power, low noise Application Specific Integrated Circuit (ASIC), designed to read out CdTe array detectors for X-γ ray imaging and spectroscopy on satellite or balloon telescopes, is presented. The chip ELBA has been realized in 0.8 μm BiCMOS technology; the front-end includes preamplifier, shaper, peak stretcher, discriminator with a dynamic range from 20 keV to 2 MeV of photon energy. The reset of the preamplifier and the high time constant of the shaper are obtained with a very compact current conveyor feedback. A multichannel prototype has been realised with a digital back-end including multiplexer, decoder, double pulse detect and logic circuitry for chip testing and calibration. The measured noise level is about 500 electrons r.m.s. corresponding to 5 keV FWHM in CdTe detectors. The total non-linearity is below ± 1.5 % and the crosstalk between two neighboring channels is about 0.7 %. The circuit is powered with a single supply at +4V with a total power consumption of 1 mW/channel.

1. Introduction

The study of X and gamma ray source in space is continuously in progress and requires the development of position sensitive spectroscopic grade detectors (PSD). Cadmium telluride (CdTe) and Cadmium Zinc Telluride ($Cd_{1-x}Zn_xTe$) have been considered being excellent semiconductors to cope the wide dynamic range from few keV up to some MeV of photon energy [1]. The proposed PSD's are pixel-type with several thousand of channels, so that low-power ASIC's are required for the read out electronics. The low-power and the spectroscopic grade requirements, in terms of noise, linearity, cross-talk immunity, are somewhat in conflict and demand for challenging circuit design. In this work we present the ASIC ELBA specifically designed to be low-power, low-noise and with a wide dynamic range in order to be employed to read out the CdTe array detectors of the CIPHER telescope [2]. The chip has been implemented in 0.8 μm BiCMOS technology of Austria Micro Systems (AMS).

2. ELBA ASIC specification

The required specifications of ELBA ASIC are: a low power consumption (<3mW/channel), a wide dynamic range (20 keV-2 MeV), linearity error <2%, shaping time 1 μs, noise: ≤5 keV FWHM in CdTe detectors, corresponding to 500 electrons r.m.s.. The front-end has to be optimised for 1 pF detector capacitance and must be able to handle detector current up to 100 nA. A version of the chip with a restricted input energy range (10 keV-100 keV) and with a noise below 2 keV FWHM will use the same architecture of the presented ASIC.

The chip design has been particularly influenced by the low power requirement, which forced to find solutions for the simplest circuit topologies assuring at the same time spectroscopic grade performance, also in terms of high thermal stability of the transfer functions.

An 8 channels prototype chip has been designed and produced in 0.8 µm BiCMOS technology of Austria Micro Systems (AMS). The chip include also a digital back-end described in section 4.

3. The analog section

3.1. The charge preamplifier

The analog part of ELBA is constituted by a charge sensitive preamplifier, a second-order semigaussian shaper, a peak stretcher and a discriminator. The design has been done for a single power supply of 4 V. The charge preamplifier employ a p-MOSFET as input transistor and bipolar transistors for having maximum transconductance at the minimum bias current. The discharge of the feedback capacitance is continuous and implemented with a current-conveyor as schematically shown in Fig. 1 [3]. Using this technique it was possible to implement an equivalent feedback resistance of 170 MΩ as far as the noise is concerned and, at the same time, to realize the first shaping time constant within the preamplifier itself. The current source I_{bias}=20 nA is necessary to bias the current mirror and determines the noise level of the front-end (500 electrons r.m.s.). Operation at lower I_{bias} values implies a noise reduction (Fig.1) but an increase of the circuit non-linearity due to the large signal operation of the current mirror. The power consumption is 220 µW.

3.2. Shaper amplifier, peak stretcher, discriminator

The shaper implements a current-mode approach and consists of a high pass filter stage feeding two 'R-lens' filter cells [4]. The peaking time is set at 1.5 µs. The power consumption is 300 µW. The peak stretcher has a power consumption of 55 µW and a good linearity (error ±0.2 %) has been measured. Figure 2 shows the linearity of the whole front-end in the range 20 keV-2 MeV of photon energy, as measured by simulating a CdTe detector.

The discriminator operates in current-mode and its threshold can be externally adjusted. Its power consumption is 360 µW. Figure 4 shows the response of the front-end (shaper and discriminator output signals) to input signals ranging from 28 keV up to 2 MeV. The gain uniformity in the 8-channels prototype has been measured: the standard deviation being 1.8 %. The cross-talk between two neighboring channels has been measured to be about 0.7 %.

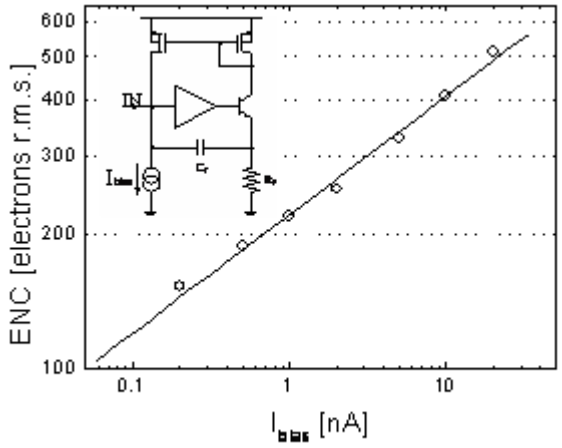
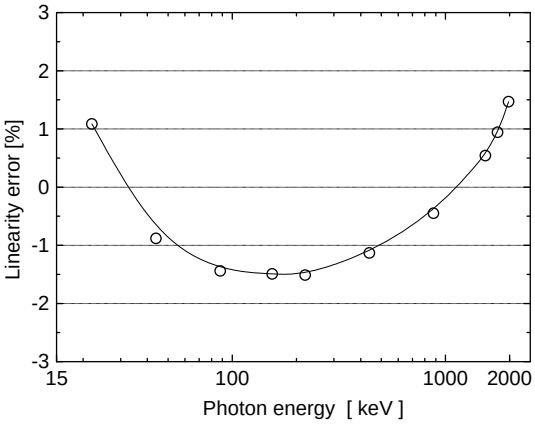
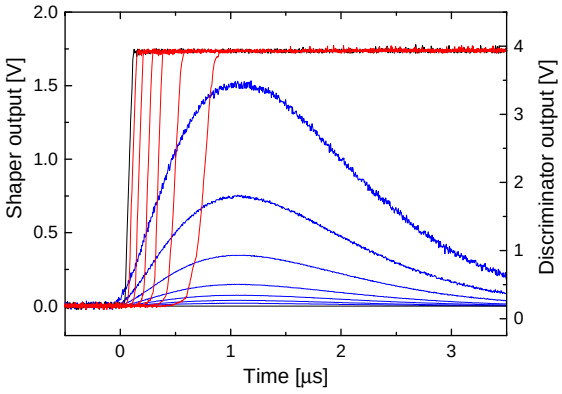


Figure 1. Equivalent Noise Charge of the front-end as function of the bias of the current mirror used to implement the continuous reset of the preamplifier.

Figure 2. Measured linearity error of the front-end.

Figure 3. Output signal of the shaper and of the discriminator for input signals ranging from 28 keV up to 2 MeV.





4. The digital section

The back end digital circuits of ELBA is constituted by an analog multiplexer driven by the discriminators of each channel. Due to the predicted low photon rate (<100 cps) simultaneous events are extremely rare, anyway accidental pile-up is detected by a double pulse logic internal circuit. An integrated encoder delivers the binary code of the triggered channel. The chip implements also a decoder and a control-logic to allow the test of each channel and the calibration of the array.

Acknowledgments

This research has been supported by the Italian Space Agency (ASI). We would like to thank S. Masci for chip packaging and bonding.

References

[1] R.B. James, T.E. Schlesinger, "Semiconductors for Room Temperature Nuclear Detector Applications", Semiconductors and Semimetals, Vol 43, Academic Press, (1995).

[2] E.Caroli, J.B.Stephen, W.Dusi, G.Bertuccio M.Sampietro, "CIPHER: Coded Imager and Polarimeter for High Energy Radiation", Nucl. Inst. Meth. A448, 2000, pp. 525-530.

[3] M. Sampietro, G. Bertuccio, "Zero Power Current Conveyor for DC Stabilisation and System Reset of Fast Current Pulse Amplifiers", Electronics Letters, Vol.34, No.19, 1998, p.1801-1802.

[4] G. Bertuccio, P. Gallina, M. Sampietro, "R-Lens Filter: An $(RC)^n$ Current-Mode Lowpass Filter", Electronics Letters, vol.35, no. 15, 1999, pp. 1209-1210.

Note

Two versions of the ASIC-ELBA have been developed.

The first one (described in the paper), including both analog and digital sections, had a dynamic range of 20-2000 keV. The operating principle is described in § 3.1 of the paper, which also explains the possibility of noise reduction by using the current mirror bias in the first amplifier stage. Output signals are delivered to the external world through an analog multiplexer.

The second one (especiallly developed for the energy range 10-100 keV) differs from the 1st one for the following features:

- only analog section (preAplifier and shaping amplifier), no digital one;
- no discriminator;
- no peak pulse stretcher;
- two eight channel amplification chains have been constructed on the same chip (max 16 channels).

The 1st and 2nd versions are completely equal with respect to the pure analog section (preAmp and shaping Amp); they differ only for the conversion gain. In the 2nd version the digital section was not implemented (no peak stretcher, no discriminator, no output MUX), while two groups of 8 channel were constructed.

Since the output voltage range is 0-1.4 Volt, the 2nd version should have a conversion factor of about 1.3-1.5 mV/keV which, at 60 keV Am241, should give a voltage output of about 0.8-0.85 Volt.

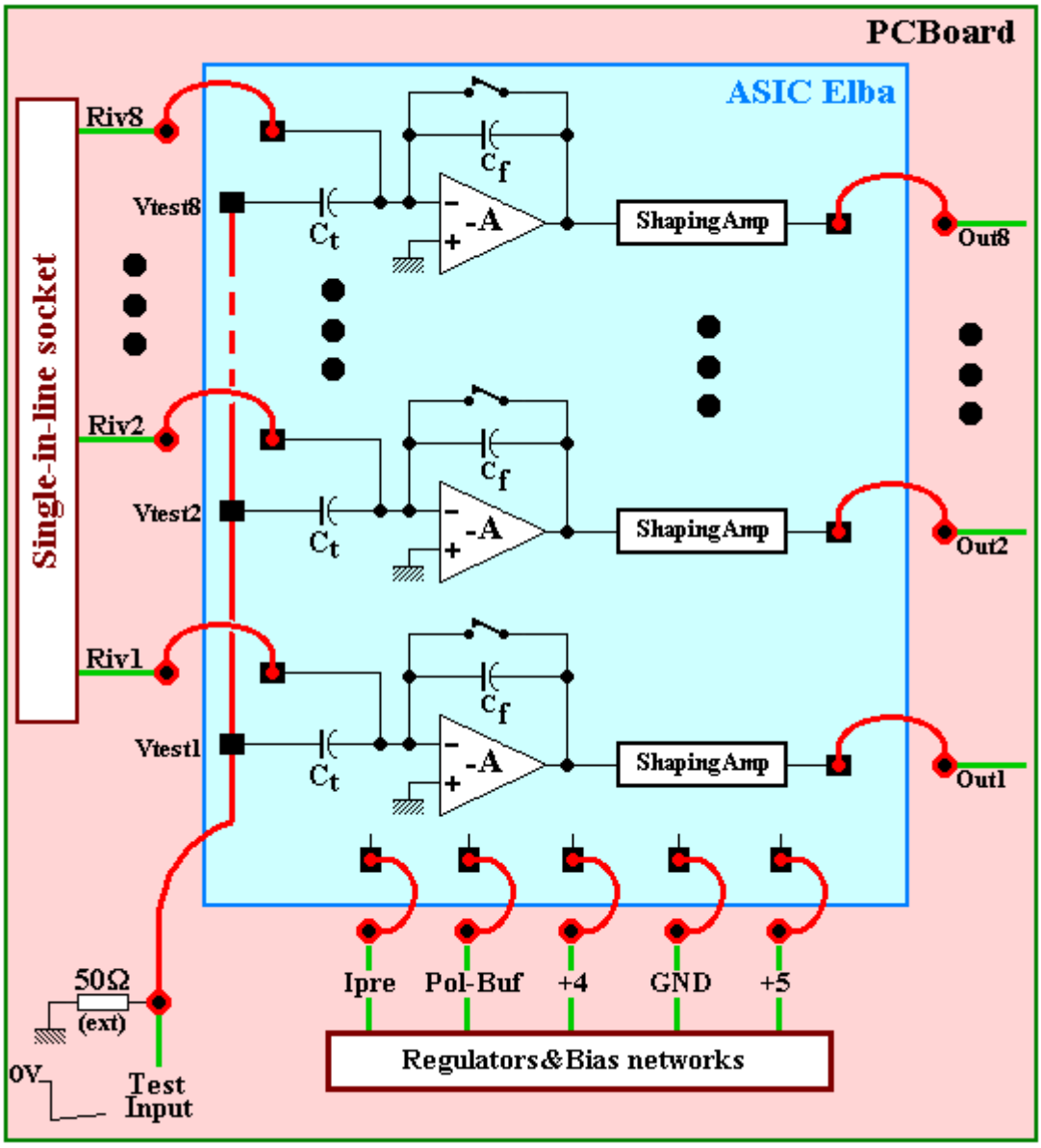
The first stage preAmp is a "reset" type charge sensitive preamplifier; this configuration is particularly used in conjunction with multi-element detector arrays in which the monocatode is biased at a negative HV while any anode (having a bias quite near to 0 V) is direcly connected to an ASIC input channel.

The CZT used should give for any anode an equivalent capacitance of 1-1.5 pF: this value could be used to simulate any anode.

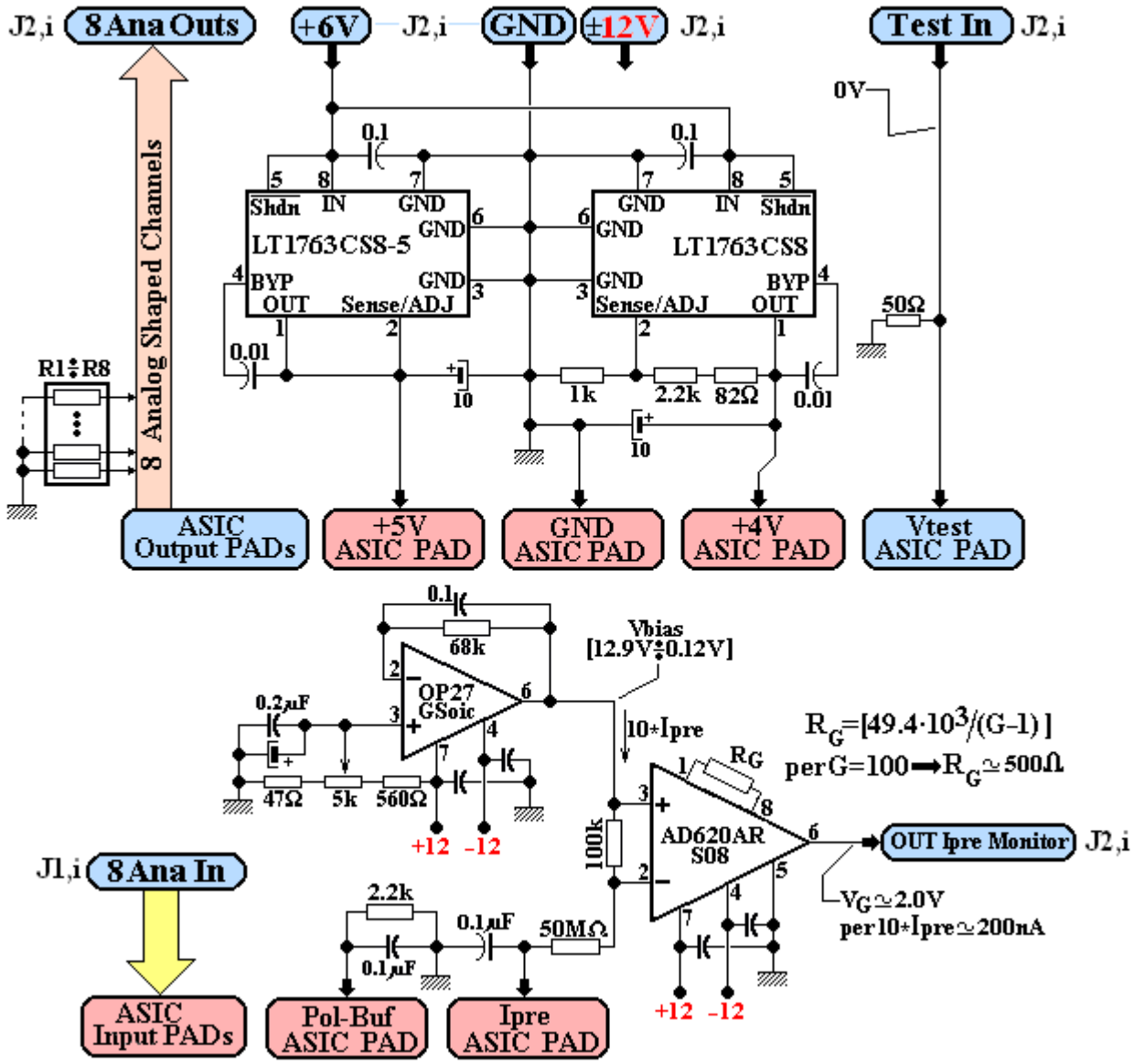
IASF-Bologna was responsible of the design and construction of the PCB. Any PCB includes:

- a modified ASIC-ELBA for the range 10-100 keV;
- a low-dropout/low-noise regulator LT1763CS83 (+4V out for the ASIC Bias)
- a low-dropout/low-noise regulator LT1763CS8-5 (+5V out for the output stages of the ASIC, i.e. for the output voltage followers)
- an OP-AMP OP-27 for the generation of the bias current of the first stage
- an Instrumentation Amp AD620 for the monitor of the bias current

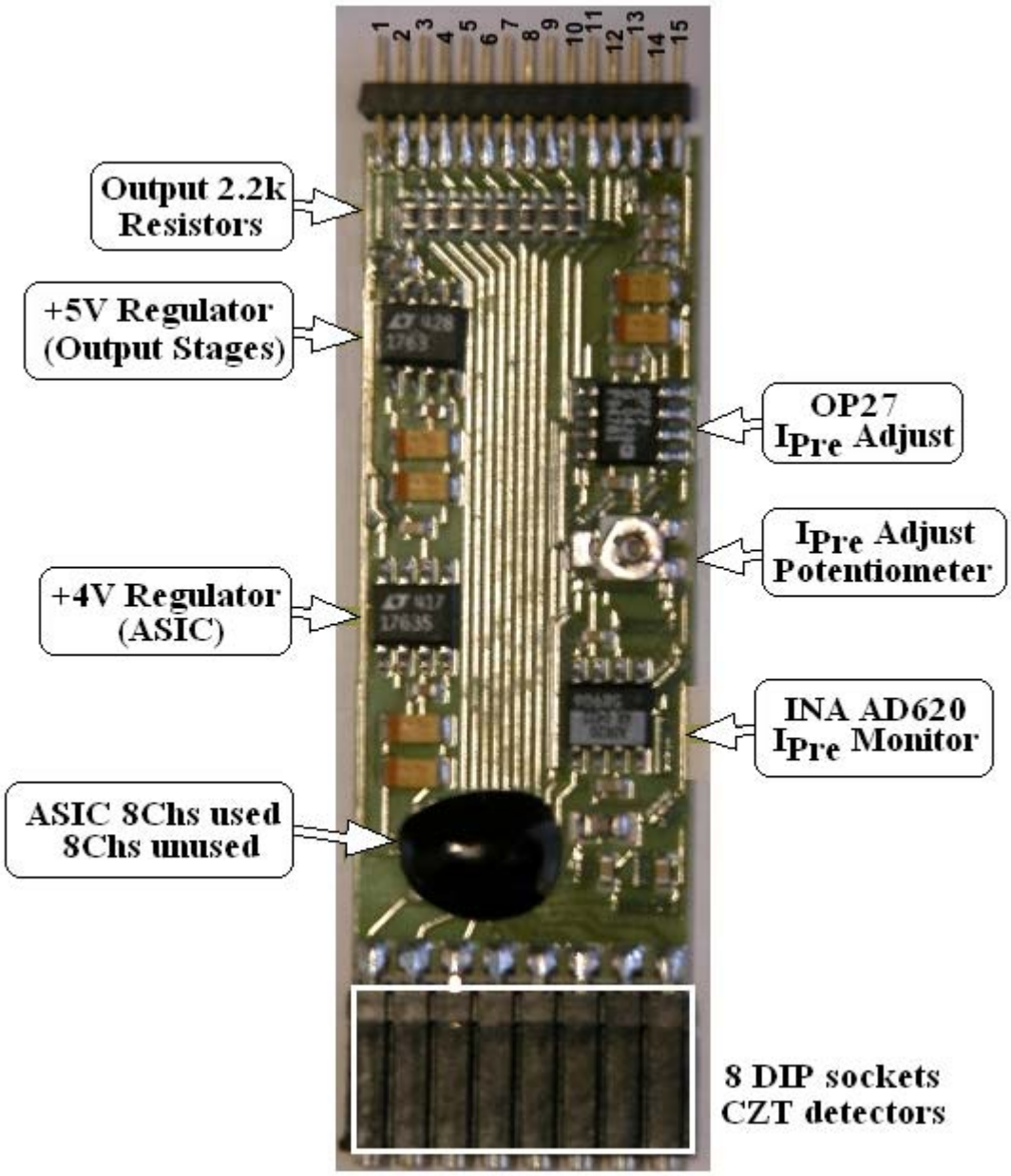
Annex 2 **8-Ch ASIC PCB: block diagram of the second version.**



Annex 3 **ASIC PCB electrical diagram.**



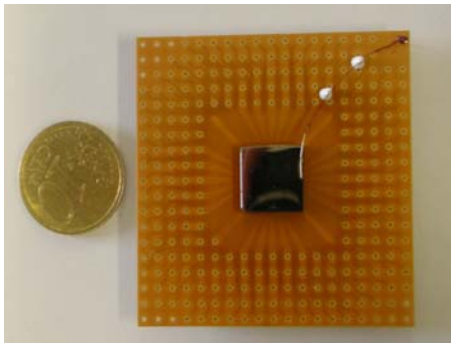
Annex 4 **ASIC PCB view with the components set in evidence.**



4. CZT Detector

The CZT detector from eV-Products (in charge of IASF-Pa) consists of an array of 256 independent pixels obtained by a segmented platinum anode deposited on a CZT single crystal. The 256 pixels array is surrounded by a guard ring, which was extended to the edge of the crystal. The guard ring is made sufficiently wide to protect peripheral pixels against surface leakage current and to reduce the influence of the edge effects. The cathode is a planar platinum electrode covering the entire detector surface. Two detectors are available, differing on thickness (1 and 2 mm); both of them have lateral dimensions of 10x10 mm^2. The CZT crystal together with the flip chip carrier board is shown in the figure of the Annex 5.

Annex 5 **Photograph of the CZT matrix; the upper surface is the monocatode.**



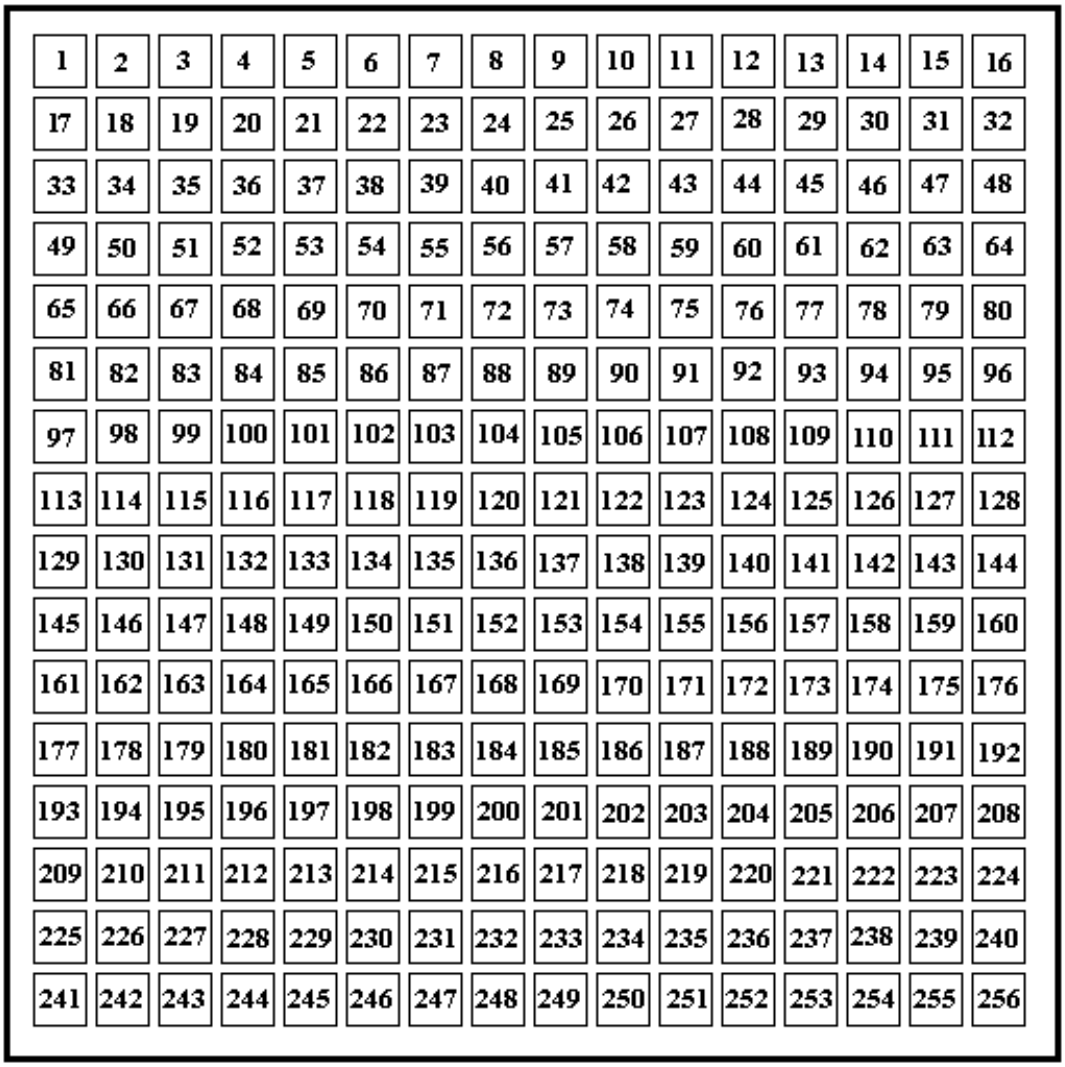
Pixel detectors	CZT (eV Products)
Geometric surface	10×10 mm^2
Active area	8×8 mm^2
Thickness	1-2 mm
Number of pixels	256
Pitch	0.5 mm (0.45 mm anodes, 0.05 mm gap)

Table 2: Detectors characteristic.

The wire connecting the cathode electrode to the bias voltage pin is clearly visible (on the right in high top corner).

Both the electrical interface and the ceramic support (vetronite PCB) are covered by a protection coating. The PCB support provides the electrical connections to the external world. The main characteristics of detectors used in this project are summarized in Table 2.

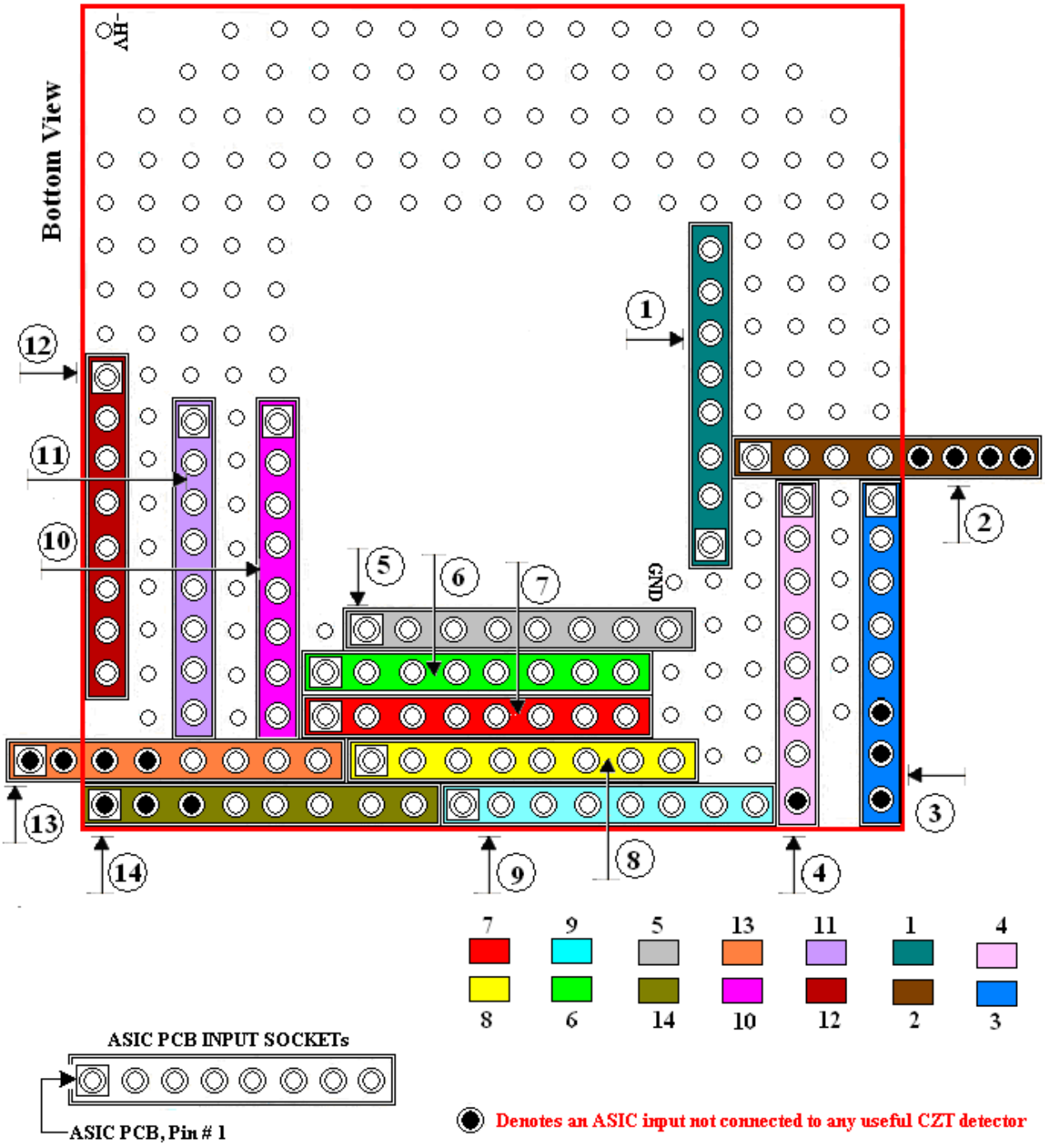
Annex 6 Schematic view of the anodes' surface for the eV 16x16 pixel CZT detector (anodes' view as it would be seen looking at the vetronite support, i.e. looking at the catode side as in Annex 5).
Pixel numbering sequence is also shown.



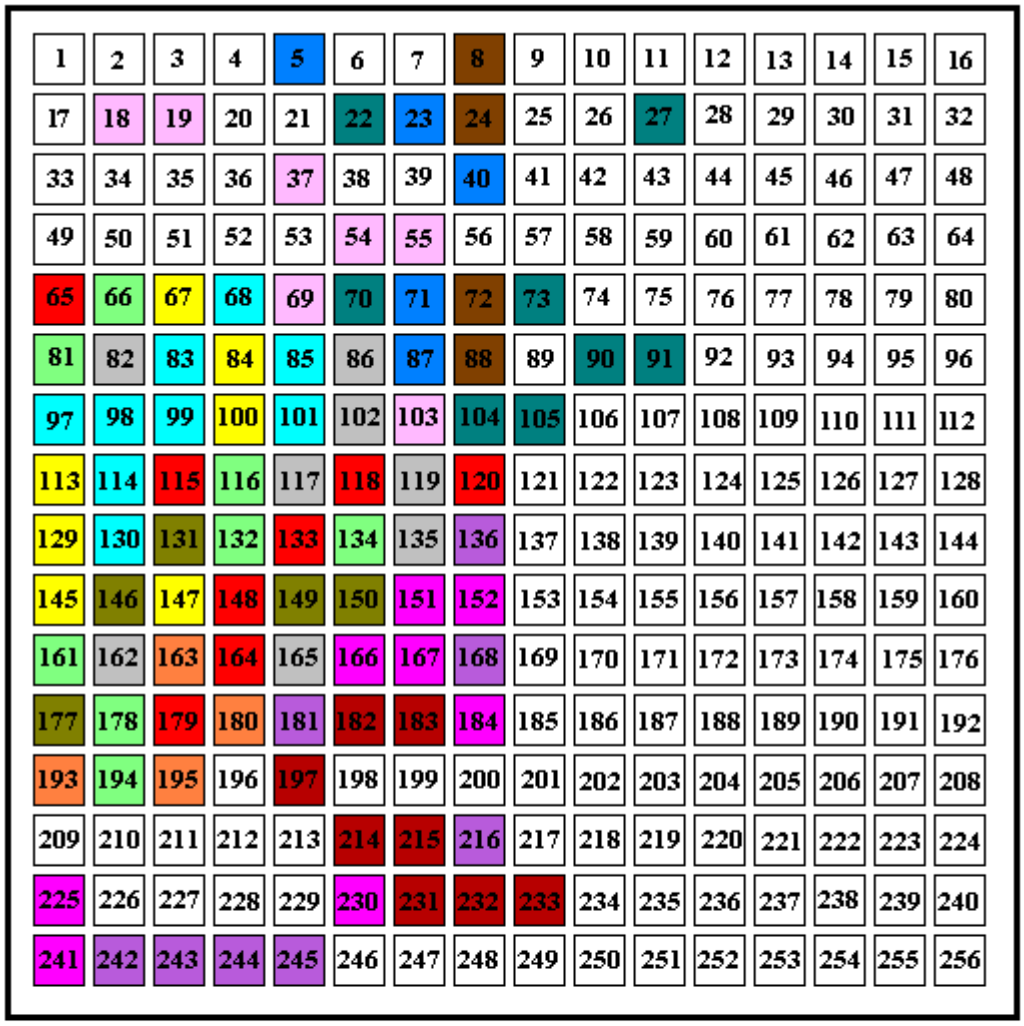
5. ASIC PCBs' distribution

The 14 ASIC PCBs' distribution permits to cover the square detector sub-array shown in the Annex 8, i.e. CZT detector pixels ranging from pix # 65 to pix # 184 distributed in rows of 8 elements by 8 columns.

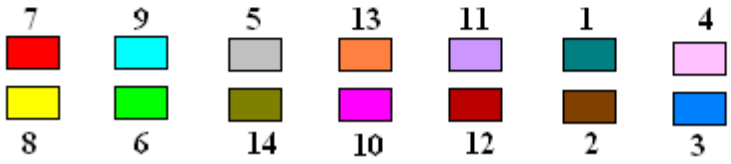
Annex 7 **Bottom view of the electrical output pad with the 14 ASIC PCBs'.**



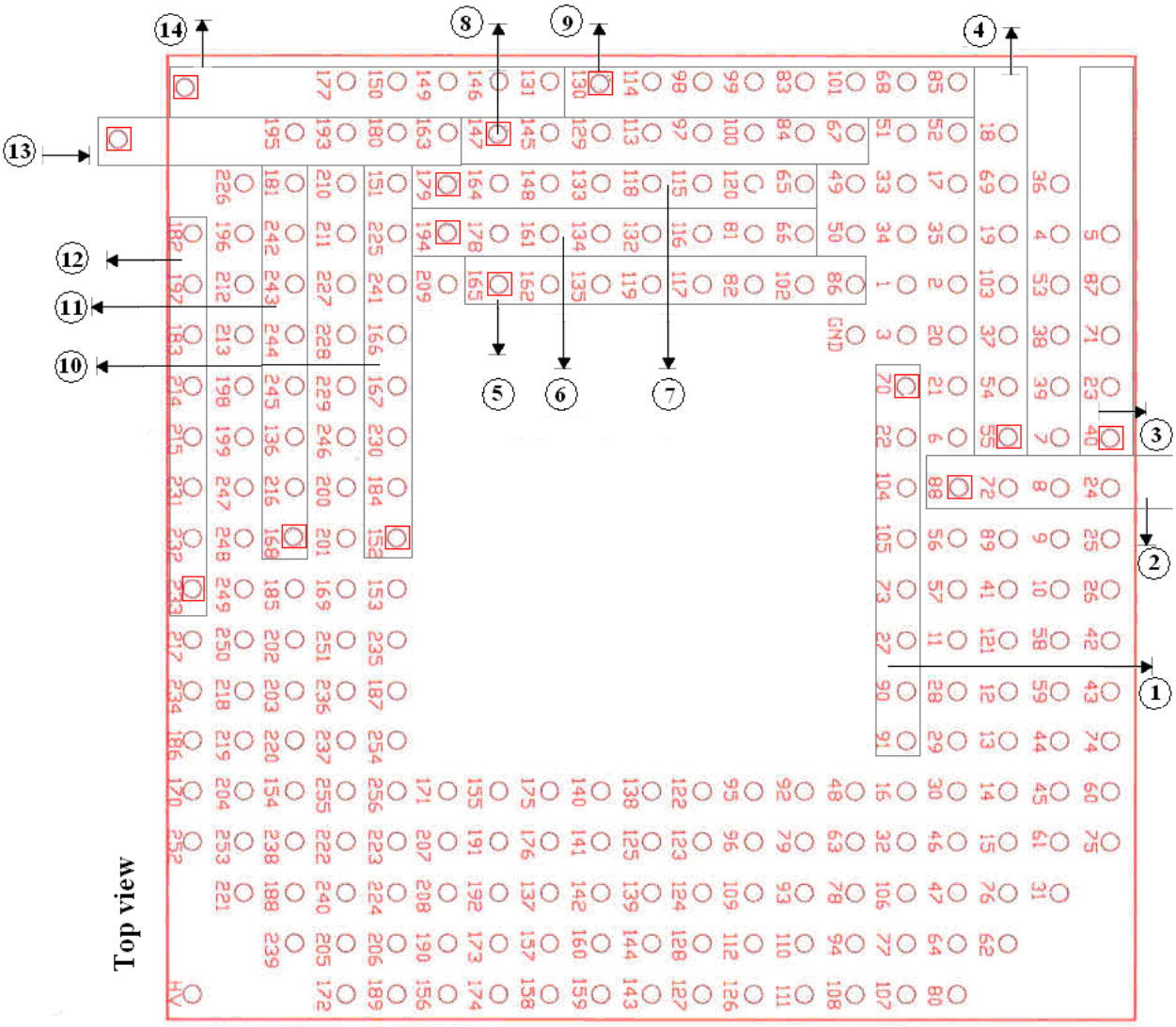
Annex 8 CZT's Anodes Coverage by using 14 ASIC PCPs'.



256 pixel CZT detector coverage with 14 ASIC PCBs'



Annex 9 **Top view of the electrical output pad together with the 14 ASIC PCBs'.**



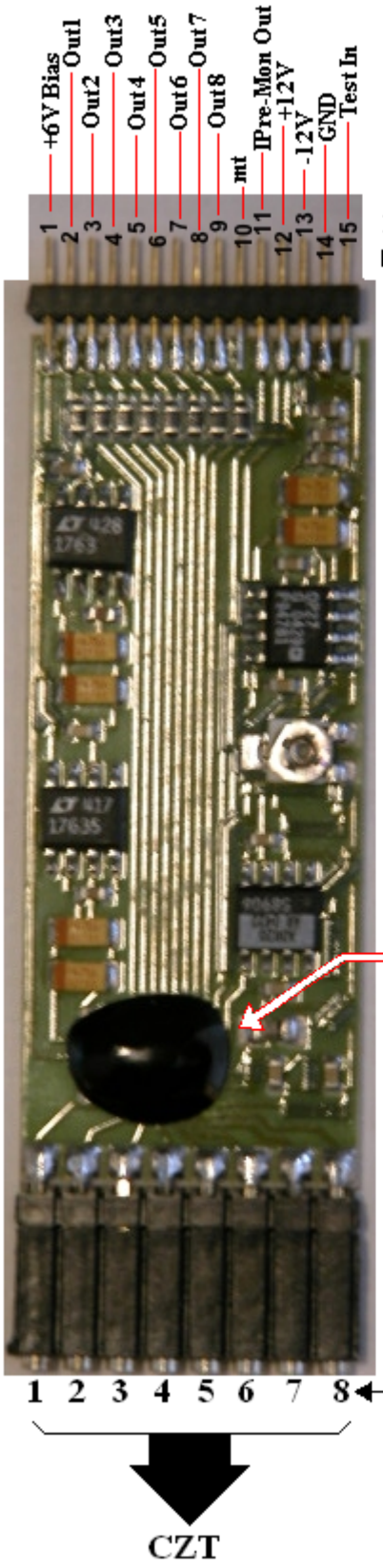
CZT detector array distribution (factory output pad): the position of the corresponding CZT pixel is found by comparision with Annex 8.

Annex 10 Correspondence between the CZT pixels and the used inputs of the ASIC PCBs'.

ASIC N.									
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
	7	179	164	148	133	118	115	120	65
	8	147	145	129	113	97	100	84	67
	9	130	114	98	99	83	101	68	85
	6	194	178	161	134	132	116	81	66
	5	165	162	135	119	117	82	102	86
	14				177	150	149	146	131
	13					195	193	180	163
	10	152	184	230	167	166	241	225	151
	11	168	216	136	245	244	243	242	181
	12	233	232	231	215	214	183	197	182
	1	70	22	104	105	73	27	90	91
	2	88	72	8	24				
	4	55	54	37	103	19	69	18	
	3	40	23	71	87	5			

Table 3. Table giving the correspondence of the CZT pixels with the relative inputs of the used ASIC PCB.

Annex 11 **ASIC PCB: Component side view.**



Input connector pins (bottom) are labelled from 1-to-8 starting from the left looking at the PCB component side.

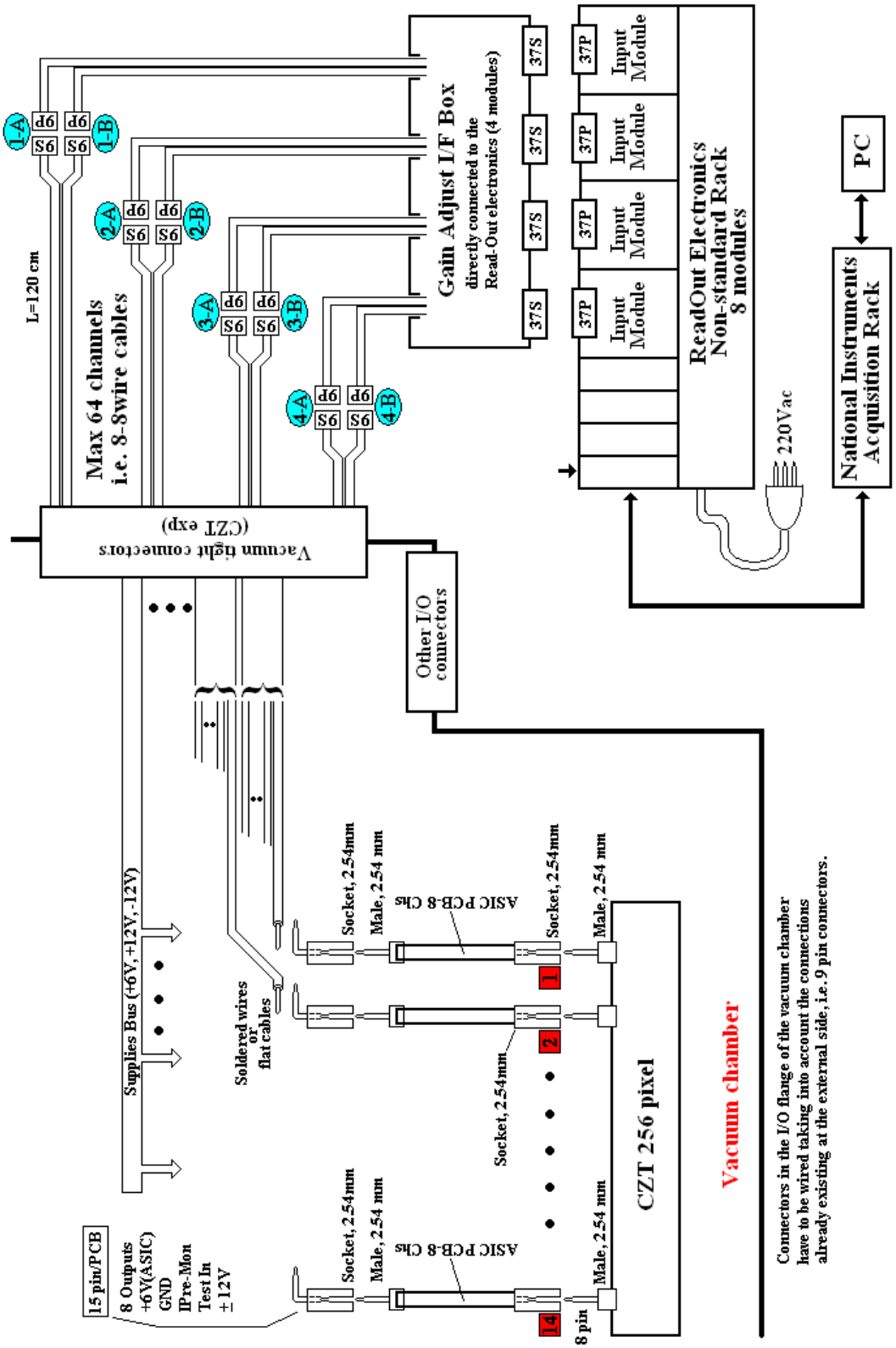
Upper connector (15 pin) provides the analog outputs, receives the bias voltages (+ 6V, ± 12 V) and supplies the I_{Pre} monitor voltage.

The DB9 pin function gives the right connections of the outputs to the gain adjust box and then to the read electronics (Takes).

DB9 P/S pin function

1	Out1
2	Out2
3	Out3
4	Out4
5	Out5
6	Out6
7	Out7
8	Out8
9	GND

Annex 12 **Experimental set up.**

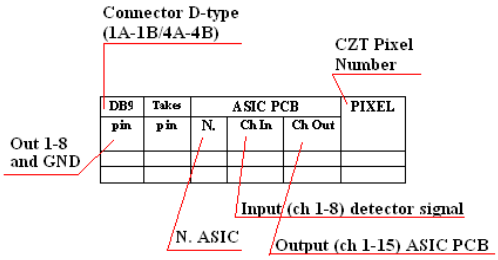


Experimental set up showing the interconnections between the ASIC PCB's and the output 9 pin connections (1A-1B, 2A-2B, 3A-3B, 4A-4B/Table 4-7).

Annex 13 **Interconnections ASIC PCB's /outputs D-type connector.**

READ-OUT ELECTRONIC BOARD

Showing physical interconnections between the ASIC PCB's outputs and the 1A-1B/4A-4B connections.



1-A	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	1	7	8	9	65
2	2	6	8	9	66
3	3	8	8	9	67
4	4	9	7	8	68
5	5	4	6	7	69
6	6	1	1	2	70
7	7	3	3	4	71
8	8	2	2	3	72
9	GND				

Table 4a/b. Board Number 1.

1-B	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch in	Ch out	#
1	9	6	7	8	81
2	10	5	6	7	82
3	11	9	5	6	83
4	12	8	7	8	84
5	13	9	8	9	85
6	14	5	8	9	86
7	15	3	4	5	87
8	16	2	1	2	88
9	GND				

2-A	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	17	8	5	6	97
2	18	9	3	4	98
3	19	9	4	5	99
4	20	8	6	7	100
5	21	9	6	7	101
6	22	5	7	8	102
7	23	4	4	5	103
8	24	1	3	4	104
9	GND				

Table 5a/b. Board Number 2.

2-B	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	25	8	4		113
2	26	9	2		114
3	27	7	6		115
4	28	6	6		116
5	29	5	5		117
6	30	7	5		118
7	31	5	4		119
8	32	7	7		120
9	GND				

3-A	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	33	8	3	4	129
2	34	9	1	2	130
3	35	14	8	9	131
4	36	6	5	6	132
5	37	7	4	5	133
6	38	6	4	5	134
7	39	5	3	4	135
8	40	11	3	4	136
9	GND				

Table 6a/b.Board Number 3.

3-B	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	41	8	2	3	145
2	42	14	7	8	146
3	43	8	1	2	147
4	44	7	3	4	148
5	45	14	6	7	149
6	46	14	5	6	150
7	47	10	8	9	151
8	48	10	1	2	152
9	GND				

4-A	Takes	ASIC	ASIC PCB		PIXEL
pin	pin	#	Ch In	Ch Out	#
1	49	6	3	4	161
2	50	5	2	3	162
3	51	3	8	9	163
4	52	7	2	3	164
5	53	5	1	2	165
6	54	10	5	6	166
7	55	10	4	5	167
8	56	11	1	2	168
9	GND				

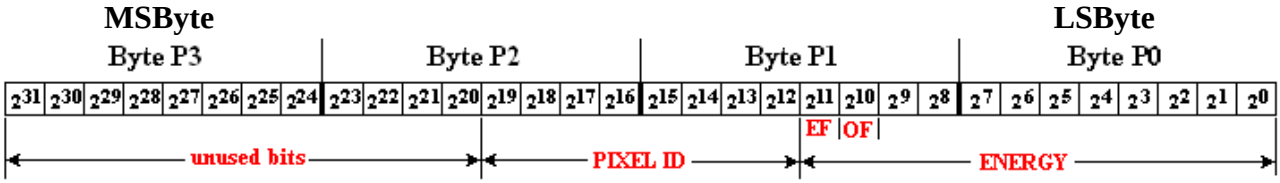
4-B	Takes	ASIC	ASIC		PIXEL
		#	Ch In	Ch Out	#
1	57	14	4		177
2	58	6	2		178
3	59	7	1		179
4	60	13	7		180
5	61	11	8		181
6	62	12	8		182
7	63	12	6		183
8	64	10	2		184
9	GND				

Table 7a/b. Board Number 4.

6. Read-Out and Data Handling Electronics (Takes)

As it can be seen from the experimental set-up (Annex 12), the shaped analog signals from the ASIC PCBs' are fed to an interface box through 8-9 pin connectors (1A-1B, 2A-2B, 3A-3B, 4A-4B) for a total amount of 64 CZT amplified channels. The I/F box, which provides an adjustement for any channel amplitude in order to fit with the input range of the analog section of the Read-Out electronics, is directly connected to Takes through 4-37 pin connectors.

Input analog signals to Takes are first processed by a coincidence-anticoincidence logic: if not more than two-three signals are present within the coincidence time (selectable between 2 and 20 μsec) they are accepted for the analysis; if more than two-three events are coincident they are rejected. In practice, any signal exceeding the low energy threshold is pre-stretched but post stretching action is issued only if the coincidence-anticoincidence rule is fulfilled. Events selected as acceptable (one or two or three within the coincidence time) have to be analyzed both in amplitude (energy information) and in interaction position (imaging information). Since the position information is directly related to the input channel of the Read-Out electronics, i.e. to the correspondence between the number of the CZT pixel and the input channel number of Takes, a position address is associated to any activated channel. If the coincidence-anticoincidence criterion is met, the amplitude(s) of the signal(s) are converted in digital by 12-bit flash Analog-to-Digital Converters. Any 12-bit converted code giving the energy information is then associated with the position code giving the interaction information: digital data are inserted in a FIFO memory from which they are red-out in the form of 32-bit parallel words. A full 32-bit data is outputted for any event, i.e. one 32-bit data for single event, two 32-bit data for two events in coincidence, three 32-bit data for three events in coincidence (multiple events).



Energy: Signal amplitude coded with 10 bit resolution (1024 energy channels).

OF: Overflow flag; when OF=1 indicates a signal exceeding the maximum energy.

EF: End of the event; EF=0 means a single pixel excitation, EF=1 multiple events.

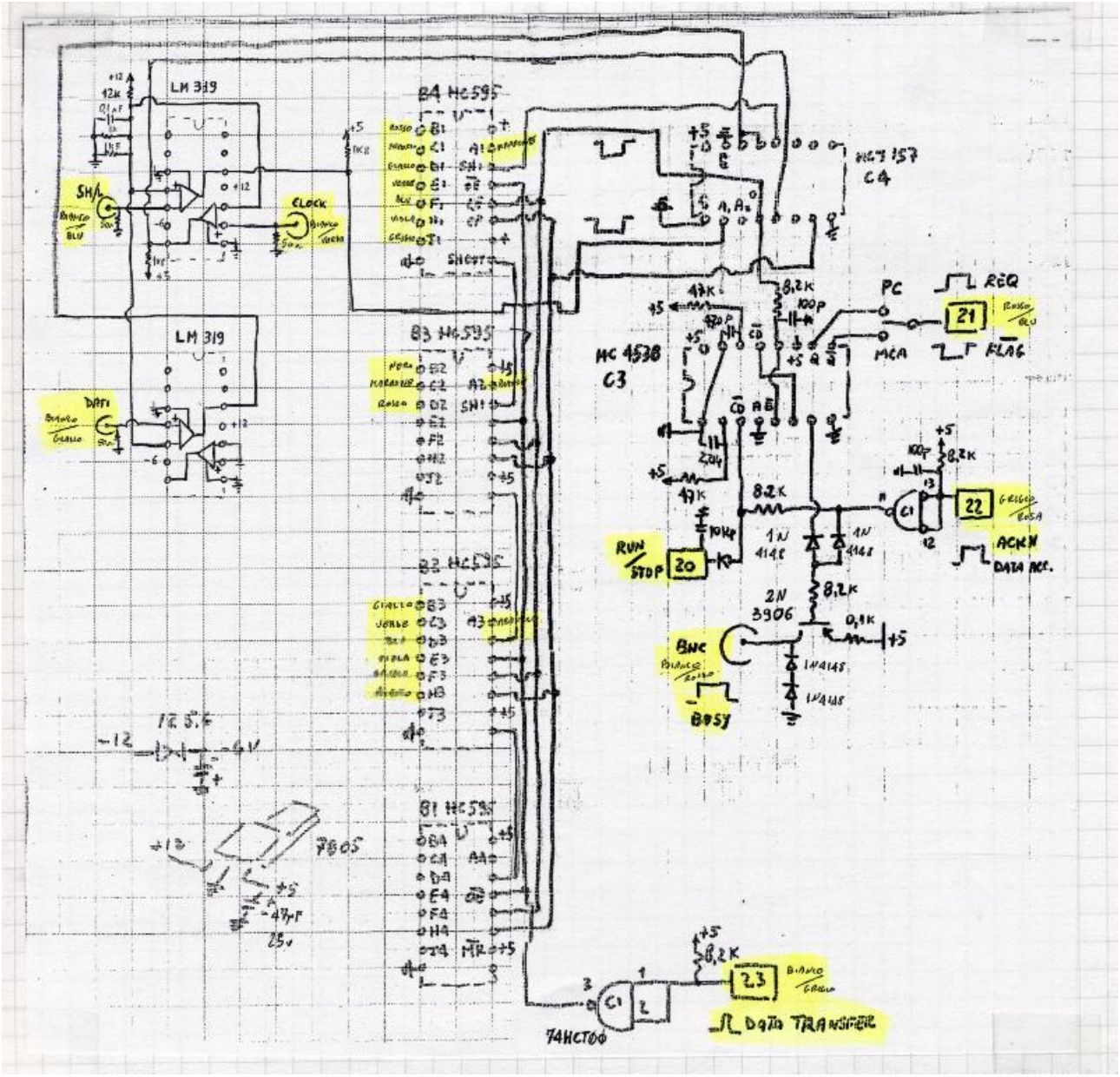
PIXEL ID: Identifies the pixel address with 8-bit resolution (only six bits are used in the present experiment to address 64 pixels).

Takes electronics is schematically divided into the following subsystems:

- **Analog input conditioning**. Up to 8 boards can be used, each of which conditions 16 analog channels by shaping CR-RC amplifiers; each amplifier is followed by a peak stretcher driven by a low energy threshold. The stretching action is extended if coincidence rule is respected. An address is associated to any input in accordance to the HW wiring, i.e. any analog input has its own address corresponding to the input pin to which it is connected;
- **Coincidence-Anticoincidence Logic** which takes the decision of how many signals are to be considered as generated by the same primary event within the a selectable time (2-20 μsec);
- Any 16 peak stretcher group is fed to a **16-to-1 analog multiplexer** whose output is connected to the 12-bit flash ADC. 10 bit are used for the energy coding;

- **Data handling board** collecting energy and address data from the distributed analog boards and storing them in an 8k FIFO memory in order to derandomize data.

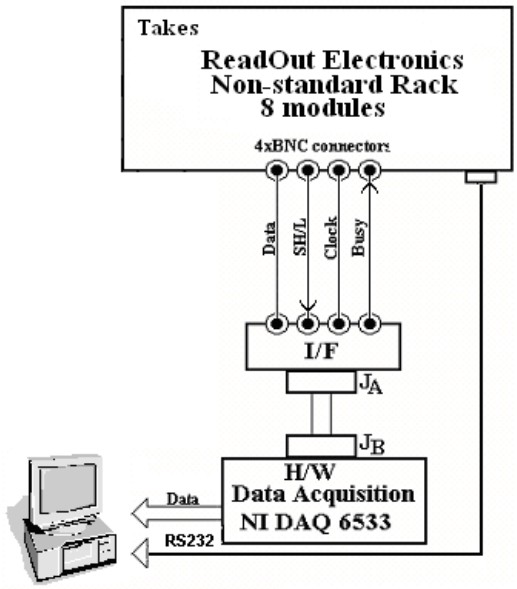
- **Output IF** which extracts data stored in the FIFO memory and presenting them for acquisition in parallel form (32-bit data words) also providing the HW acquisition commanding signal (flag) and handling the "data acknowledge" to synchronize the data acquisition subsystem.



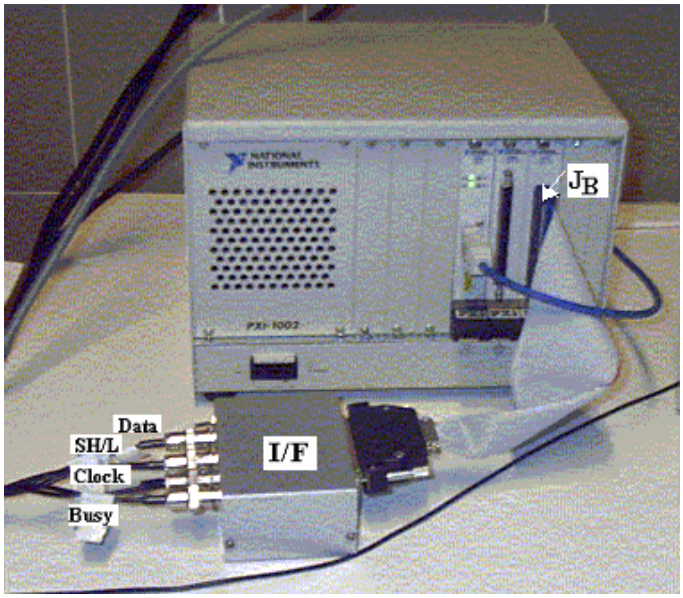
Output IF electrical diagram.

The Output IF box is physically external to Takes electronics, being wired in an independent box. It is connected to Takes by means of four coaxial cables:

- **Serial Data**,
- **Clock** at 5 MHZ,
- **SH/L** shifting or loading data and
- **Busy** which prevents the system from saturation.

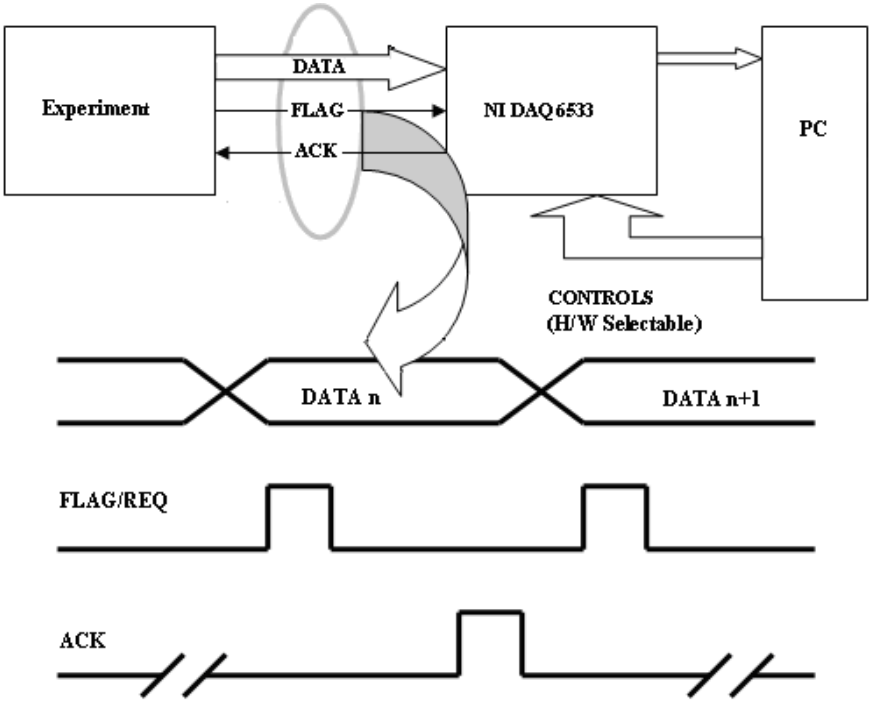


Block diagram digital acquisition.



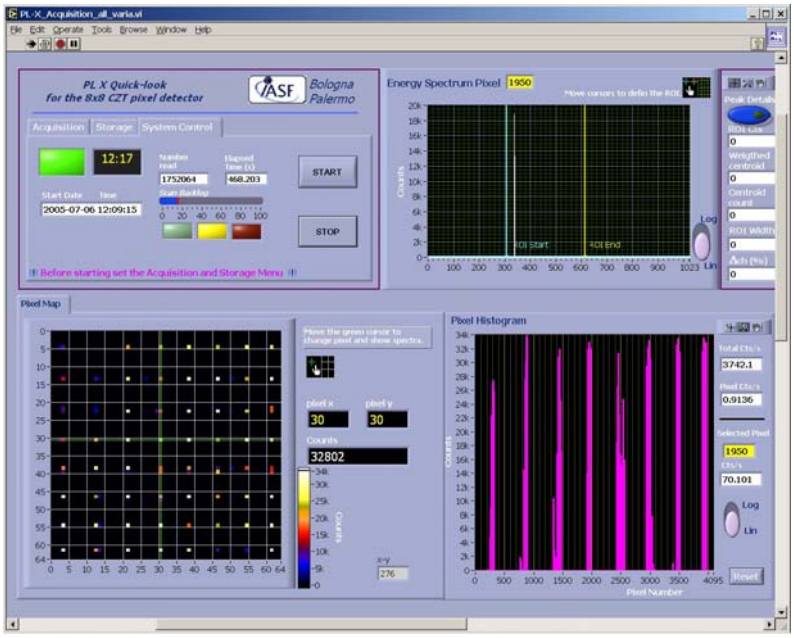
NI 6533 digital card and Output IF box.

Data are acquired by the PC through a National Instrument NI DIO 6533 digital interface which is managed by a HW handshake and directly connected to the Takes Output IF.



Handshake Takes/DAQ NI 6533.

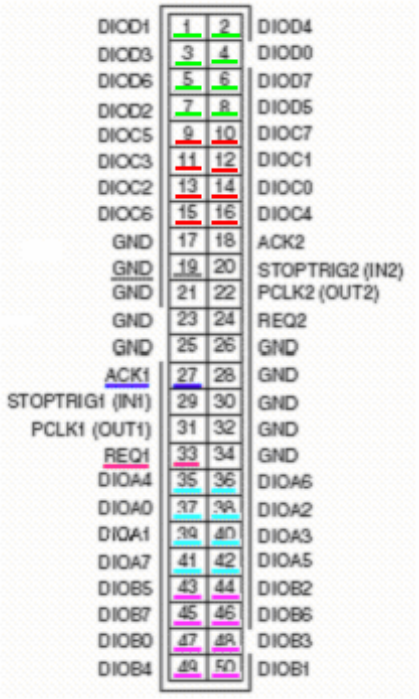
The PC resident SW (document PLX-IASF-001) is able to manage the experiment and to output both energy and position data, as well data storage. It also set up the system initial calibrations (gain correction factors, zero and offset parameters), as well as the energy window levels.



CZT SW Acquisition

Input data to the NI 6533 digital card is performed by means of a clamping 50 pin HW adaptor which, in turn, connects to the NI acquisition system through a 68 pin factory wired connector.

The pin function of the 50 pin (JB) input adaptor is shown.



68/50 Adaptor JB connector.

Port Combinations and bit Data.

DIOA0(LSB)-DIOA7(MSB): data byte P0
DIOB0(LSB)-DIOB7(MSB): data byte P1
DIOC0(LSB)-DIOC7(MSB): data byte P2
DIOD0(LSB)-DIOD7(MSB): data byte P3

Transfer Width	Possible Port Combinations	Timing Controllers That Can Be Used
32 bits	Port 0, Port 1, Port 2, Port 3	Group 1

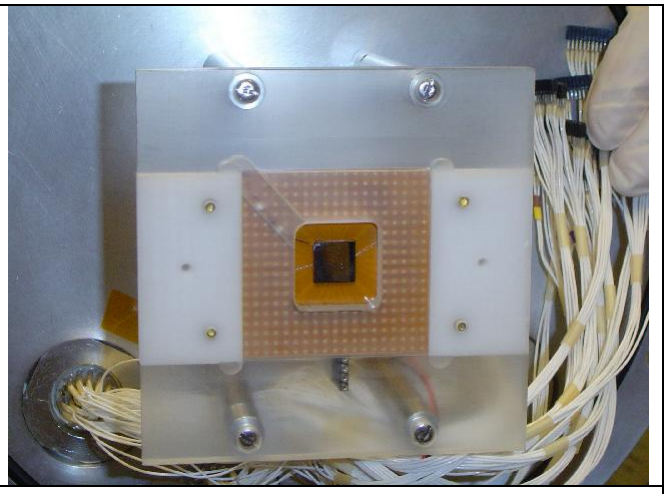
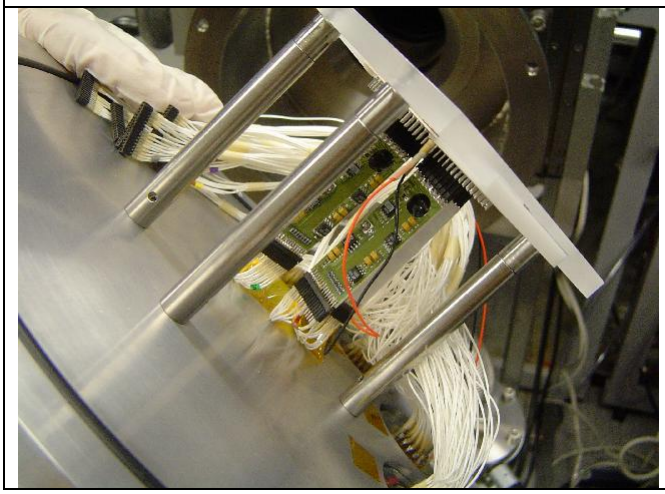
Table 8. Port Combinations NI DAQ board.

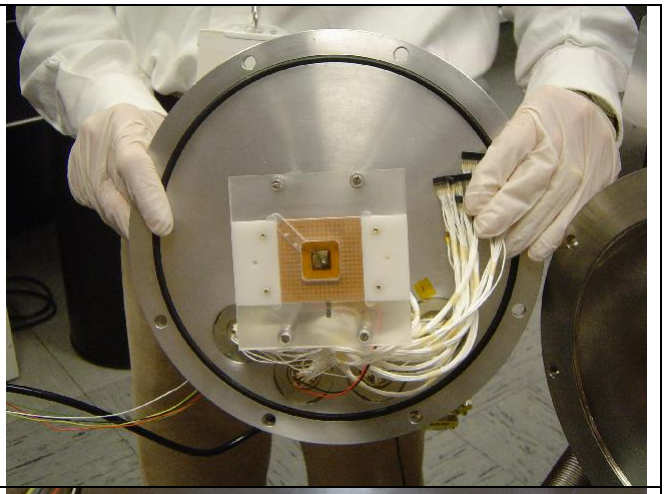
7. Leicester logbook 25-29 July

The IASF Bologna and Palermo groups in Italy together with the University of Leicester, Space Research Centre, have initiated a collaborative instrument development programme to build a hybrid position sensitive detector consisting of a Cadmium Zinc Telluride (16x16 pixel array) and a thinned EPIC CCD22. This detector would be sensitive over the 0.2 to 100 keV energy range. The aim of the collaboration is to produce a breadboard model that could be exploited in a future X-ray astronomy mission opportunity. The development of this breadboard model would place this team in an advantageous position to bid for financial support.

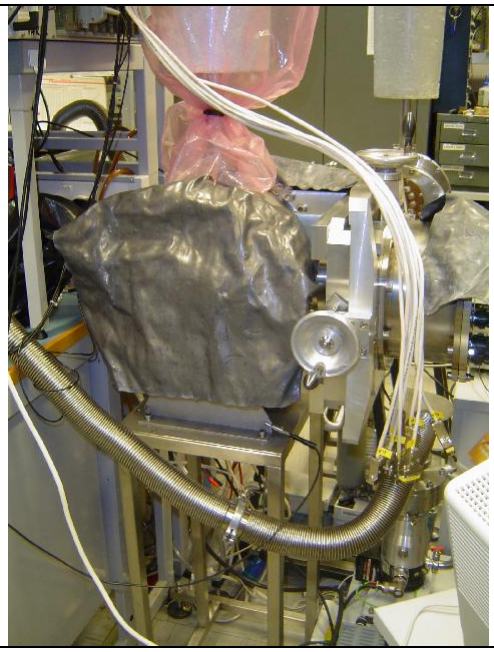
The readout electronics for the CZT detector include an ASIC based system developed by the Politecnico di Milano, Italy in collaboration with LABEN, Italy.

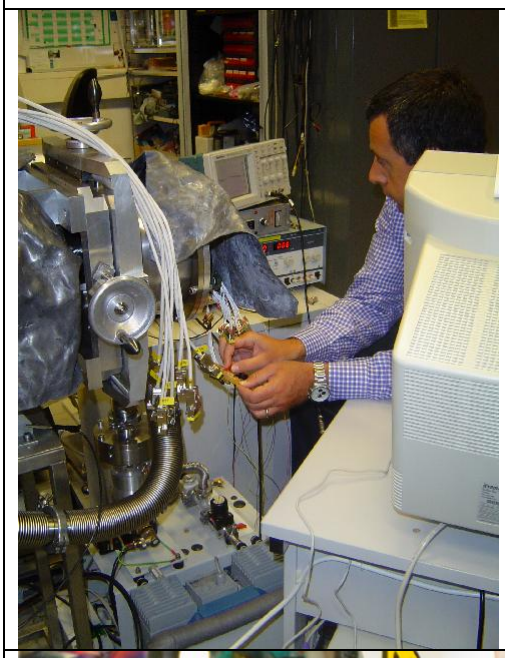
A collaborative experimental programme has been defined to, integrate the two detectors in a specifically designed facility at the University of Leicester and carry out a series of live X-ray tests over the sensitive range of the detector. Technical challenges to resolve include: a reduction of the system noise and testing of all the ASICS designed for the CZT detector.

Front view of the CZT pixel detector on the plexiglass support and vacuum interface cables built by the Leicester Group. *26 July 2005* (Mechanical Integration).	
	Internal view of the overall detector system (CZT pixel array and ASIC) attached to the vacuum flange. On *28 July 2005*, we mounted ASICs nos. 1, 2, and 5. On *30 July 2005* we mounted ASIC no. 7 for the single test.

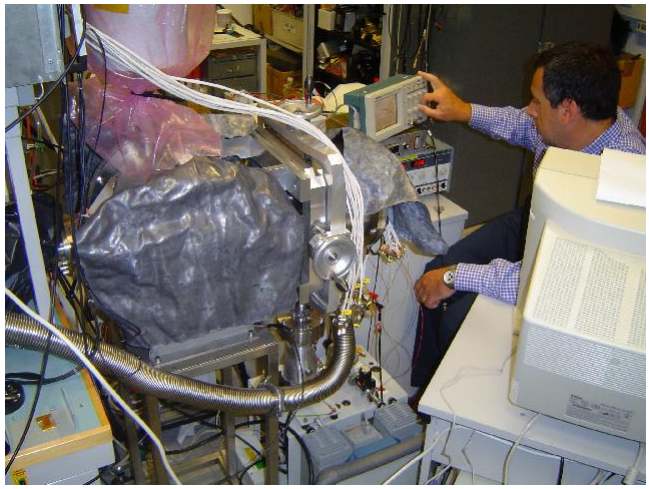
The detector is supported on the vacuum flange by four aluminium posts.	
Flange external view with the 4 vacuum tight connectors and cables to the Takes Electronics.	
	Overall view of the vacuum chamber containing both the CCD (rear) and the CZT pixel detectors. In the picture both the vacuum pump and the CCD cooling system with liquid N (top) dewar are visible.

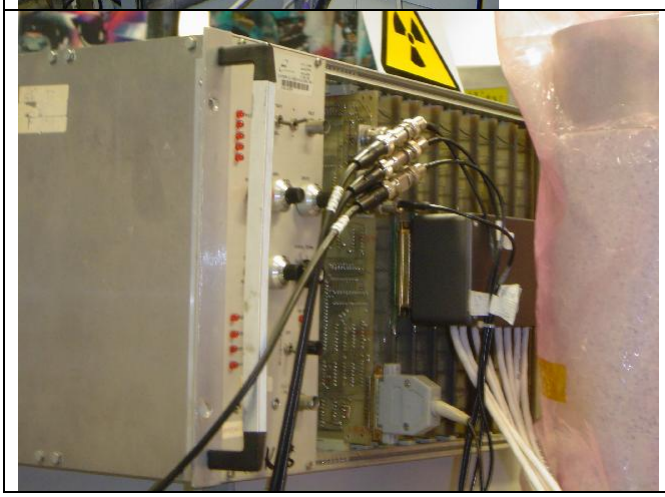
The detector chamber covered with lead foil during testing with an ^{241}Am source.
At the rear the CZT x-y translation stage is visible.
This facilitates the alignment of the CCD with the CZT detector.





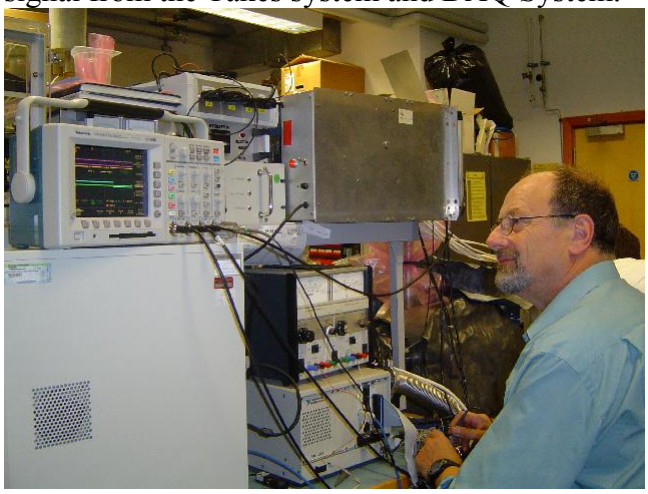
Test of the signal outputs directly from the ASIC board.

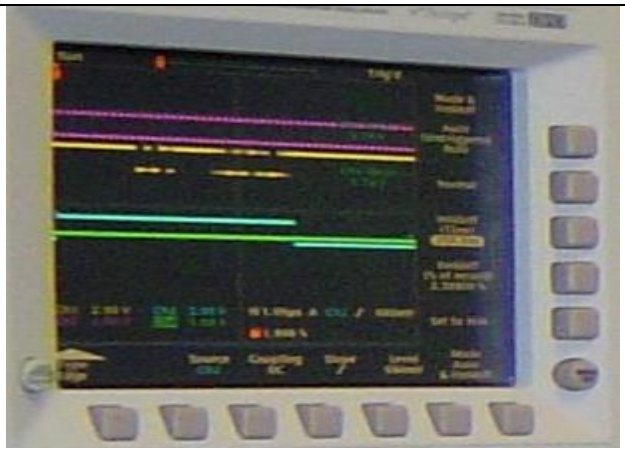




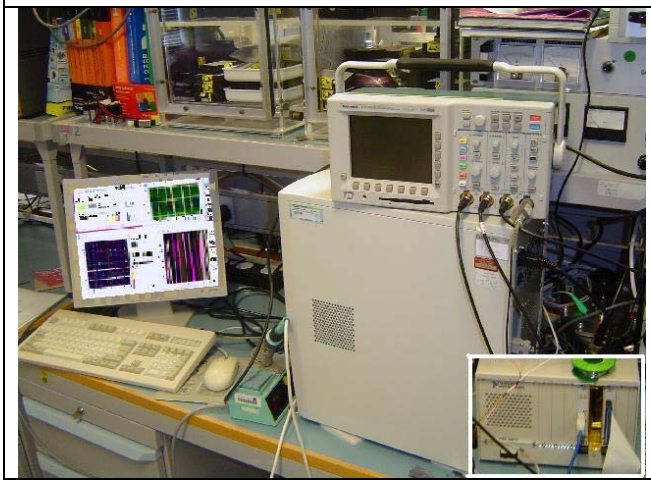
64 channel Takes Electronics with the interface box connected to the ASIC output and the four coaxial cables with the output data on protocol signals.

Test of the interface between the coaxial cable signal from the Takes system and DAQ System.





The picture shows the outputs from the 4 coaxial cables: **Serial Data**, **Clock** at 5 MHZ, **SH/L** shifting or loading data and **Busy** signal, which prevents the system from saturation.



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