Characterization of a pixel CZT detector coupled with the modified ELBA ASIC readout device

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1. Aims and summary

This document reports the results of the measurements performed on an X-Ray detection system based on a 16x16 pixel CZT array from eV products and a custom readout ASIC.

In particular, the performance of the ASIC were investigated in order to characterize the operative features of the front-end active device of the detection equipment, mainly for future applications. The results of the tests carried out should also represent a guide in preparation of the experiment which is being arranged in collaboration between the Leicester University Space Research Center and INAF/IASF Institute. This experiment should assemble a hybrid detector prototype based on a soft X-ray detector (a spare CMOS CDD of the EPIC/XMM developed at Leicester University) and a CZT 16x16 pixel detector, available at IASF/INAF, with custom ASICs (developed in collaboration with Politecnico of Milano) as analog front-end electronics. A brief description of the expected goals and of the set-up of the combined experiment can be found in the Hybrid Exp reference below reported.

***Applicable Documents*:**

Acronyms	**Title**
CZT1	S. Del Sordo et al., *Characterization of a CZT Focal Plane Small Prototype for Hard X-Ray Telescope,* IEEE Trans On Nucl. Sci., in publication (2005)
ASIC1	G Bertuccio et al., *Low power BiCMOS ASIC for wide energy range X-gamma ray imaging and spectroscopic detectors,* Nucl. Instr. and Meth., A508 pp. 465-467 (2004)
ASIC2	J. Stephen et al., *Development of a CZT/CdTe focal plane prototypes for hard X Ray optics", Private communication*
Hybrid Exp1	Abbey et al., *CZT Bo/Pa Se- up for the hybrid experiment at the Leicester University* IASF/Bo Internal Report n. 425/2005
CCD1	P.J. Pool, R. Holtom, D.J. Burt, A.D. Holland *Developments in MOS CCDs for X ray astronomy,* Nucl. Instr. and Meth., A 436 pp 9-15 (1999)
CCD2	A.D. Short, R.M. Ambrosi, M.J.L. Turner *Spectral redistribution and surface loss effects in Swift XRT (XMM-Newton EPIC) MOS CCDs* Nucl. Instr. and Meth., A 484 pp 9-15, pp 211-224 (2002)

2. The laboratory set-up

The detection equipment consists of two main components:
<u>CZT detector (eV Products)</u>:
10x10 mm^2, 2 mm thick, 16x16 pixel array, segmented anode with pixel size of 0.45x0.45 mm^2, monocathode biased at –200 V [CZT-1]

<u>ASIC-ELBA</u>:
Two versions of the ASIC-ELBA have been developed. The first one including both analog and digital sections, had a dynamic range of 20-20000 keV [ASIC-1]. The second one (especiallly developed for the energy range 10-100 keV, [ASIC-2]) differs from the 1st one for the following features:
- only analog section (Charge preAplifier and shaping amplifier), no digital one;
- no discriminator;
- no peak pulse stretcher;
- channel conversion factor (overall gain).

The five available ASIC PCBs were labeled as:
- PCB “A”
- PCB “B” not usable (see below)
- PCB “C”
- PCB “D”
- PCB “E” not usable (dead, no channel out)

The ASIC PCB pair [(PCB “A”-PCB “C”) has been connected to the CZT anode output pad for a total of 16 (nominal) pixel readout.
The PCB “A” has been connected in position 6 [see pixel coverage in Hybrid Exp-1 and Fig. 19] for a readout of the pixels 194, 178, 161, 134, 132, 116, 81, 66.
The PCB “C” has been connected in position 1 [see pixel coverage in Hybrid Exp-1 and Fig. 19] for a readout of the pixels 70, 22, 104, 105, 73, 27, 90, 91.
The PCB “D” has then been connected in position 6, in place of PCB “A”; later on in position 7 (Fig. 19) for the readout of pixels 179, 164, 148, 133, 118, 115, 120, 65.

Fig. 1 shows the wiring of the ASIC PCB “A” to the CZT output pad.
Fig. 2 shows the arrangement of the two boxes housing the detector and the bias voltage regulators, respectively.
Fig. 3 shows the overall thigh light housing used to perform the measurements and to provide the electromagnetic shielding from the laboratory environment.

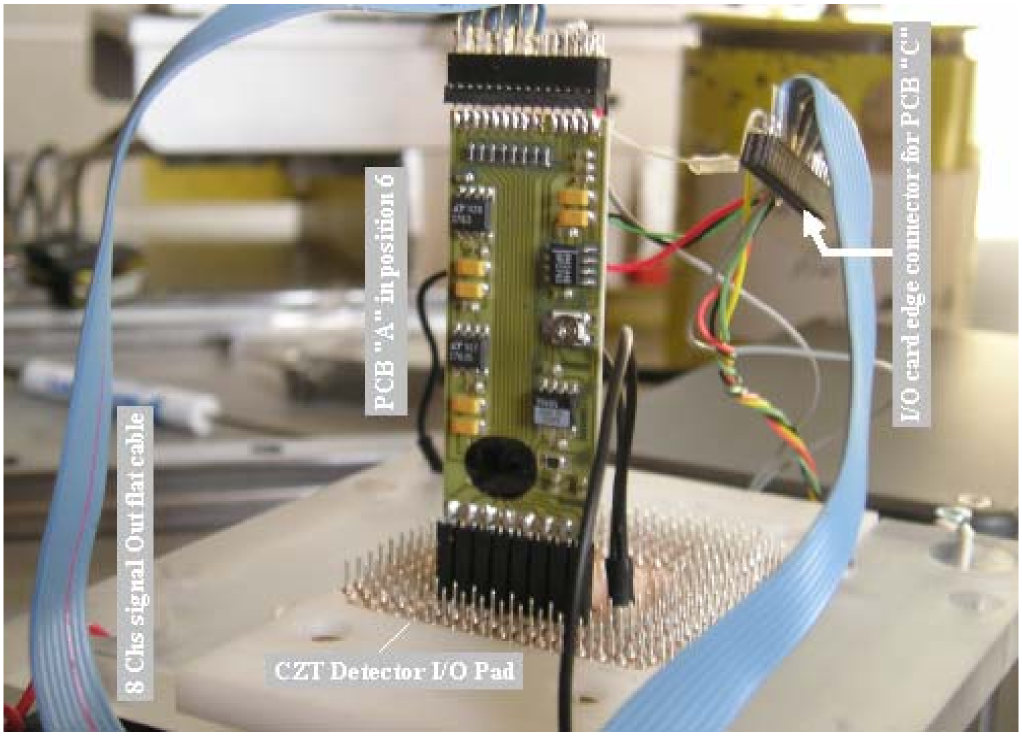

Fig. 1. ASIC PCB ”A” coupled to position 6 of the CZT anode output pad.

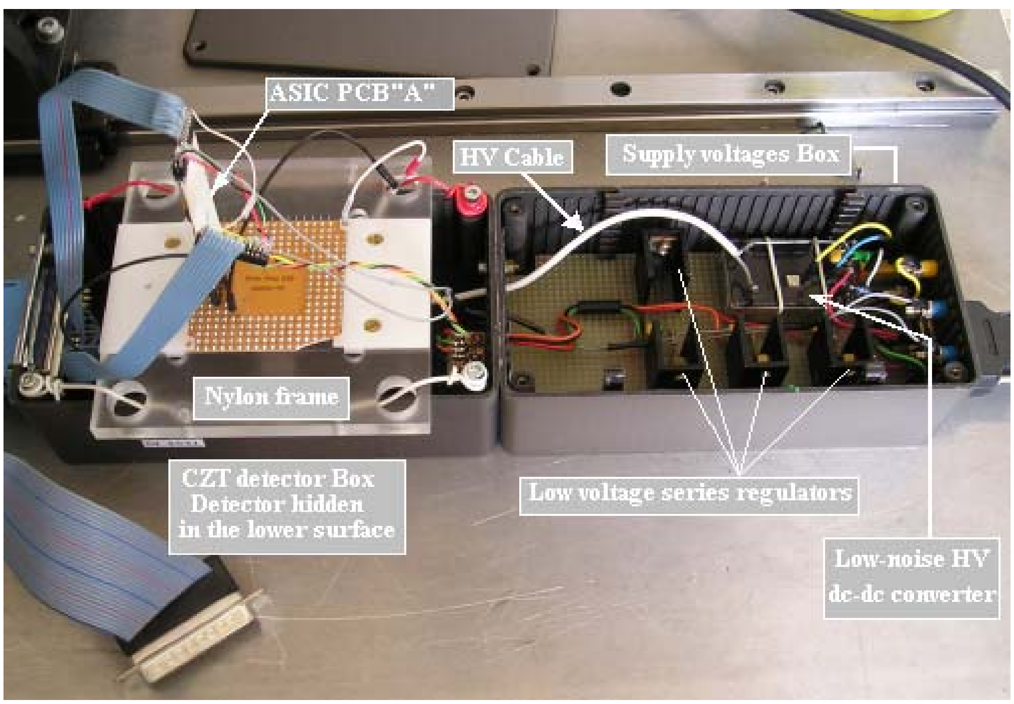

Fig. 2. Mechanical coupling of the CZT detector Box (left) and the bias voltage Box (right). The ASIC PCB ”A” (top left corner) is coupled to the position 6 of the CZT anode output pad.

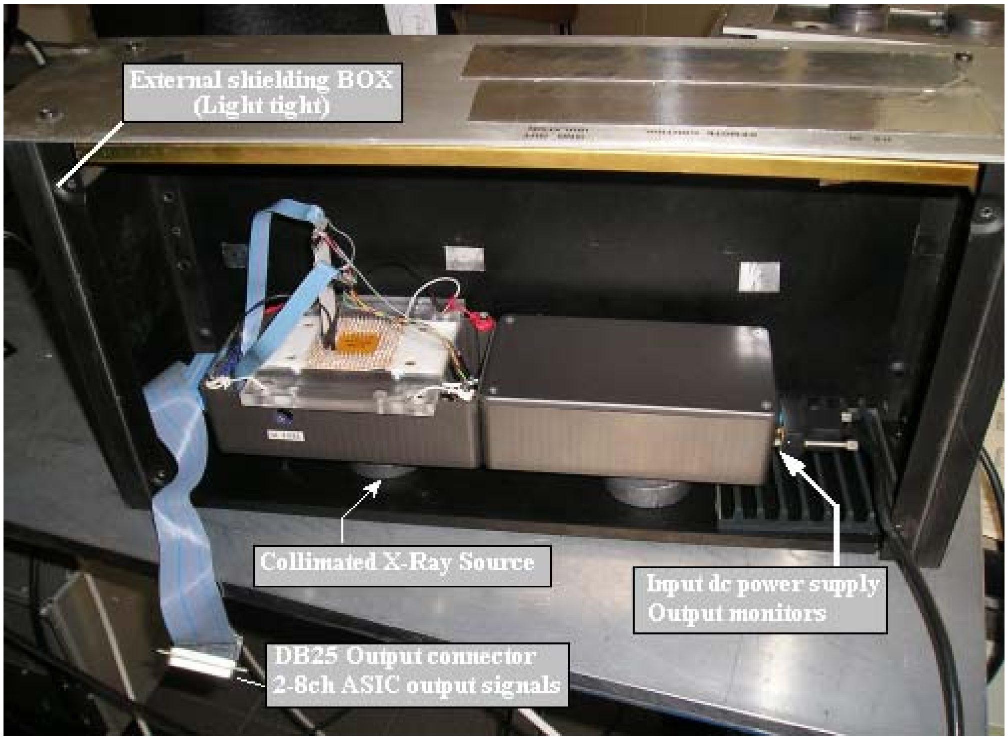

Fig. 3. Experimental set-up: the CZT and the Bias voltage Boxes, linked together, are placed in a light tight metal container.

Since any ASIC output channel has a DC offset voltage of about 1-1.5 V, which also depends on the I_{Pre} regulation [ASIC-1, ASIC-2], it was required to eliminate this DC output voltage before further processing the analog data with a Multichannel Pulse Height Analyzer (MCPHA).

For any ASIC channel the same amplification chain has been used in the measurements as shown in Fig. 4.

Since the second version of the ASIC was not intensively tested after fabrication, the first demand was to improve the knowledge of the performance of the ASIC mainly for what concerns the possibility to reduce the noise by acting on the bias current (I_{Pre}) of the first amplification stage.

The PCB "A" pixel # 116 was chosen as initial test element. PCB "B" was discarded since it did not permit any I_{Pre} regulation. The MCPHA Aptek is the main storing data equipment; off-line analysis of stored measurement data has been performed under control of the Aptek SW.

3. First set of tests on a single ASIC channel.

The CZT cathode was irradiated with a ^{109}Cd X-Ray emitting source and data were accumulated from pixel # 116 (ASIC PCB "A", channel # 6) at various I_{Pre} values. The off-line analysis has been performed on both the variation of the voltage corresponding to the ^{109}Cd 88 keV peak and the energy resolution at the same energy. Resulting data are summarized in Table I.

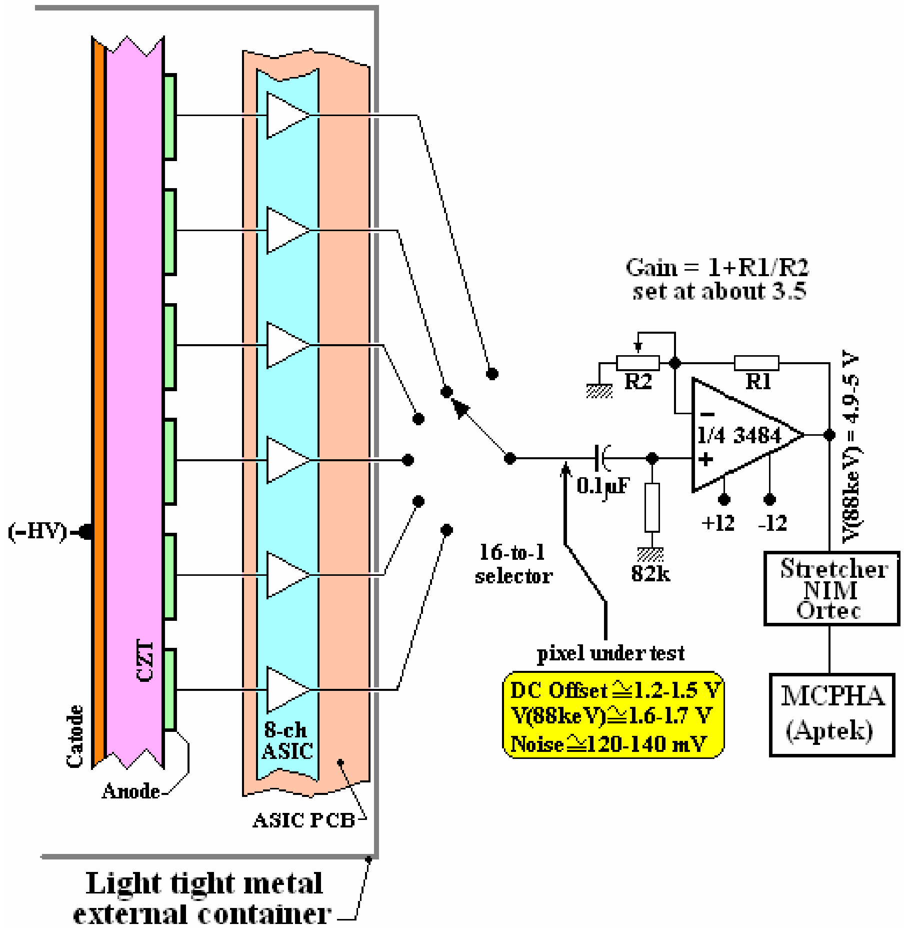

Fig. 4. Analog processing set-up used for most of the data collection and storage.

Table I. CZT Pixel #116, ASIC PCB "A" in position 6.

I_{Pre} (nA)	88 keV peak (centroid, ch #)	Resolution(%)	Filename
6.10 V	733.03	4.9	Cda2
5.08 V	752.85	4.8	Cda3
4.12 V	774.34	4.7	Cda4
3.08 V	801.78	4.5	Cda5
2.08 V	835.10	4.2	Cda6
1.01 V	884.45	3.8	Cda7
0.51 V	916.97	3.3	Cda8

As expected [see ASIC-1, ASIC-2], by decreasing the the bias current of the preamplifier 1st stage, I_{Pre}, the noise contribution (FWHM) improves and the signal amplitude increases (Fig. 5).

In the tested range, $\Delta I_{Pre} \cong [0.5 \div 6]$ nA, the energy resolution improves with a mean coefficient of about –0.29%/nA, while the 88 keV position highers in the mean of about 33 chs for any 1 nA increment.

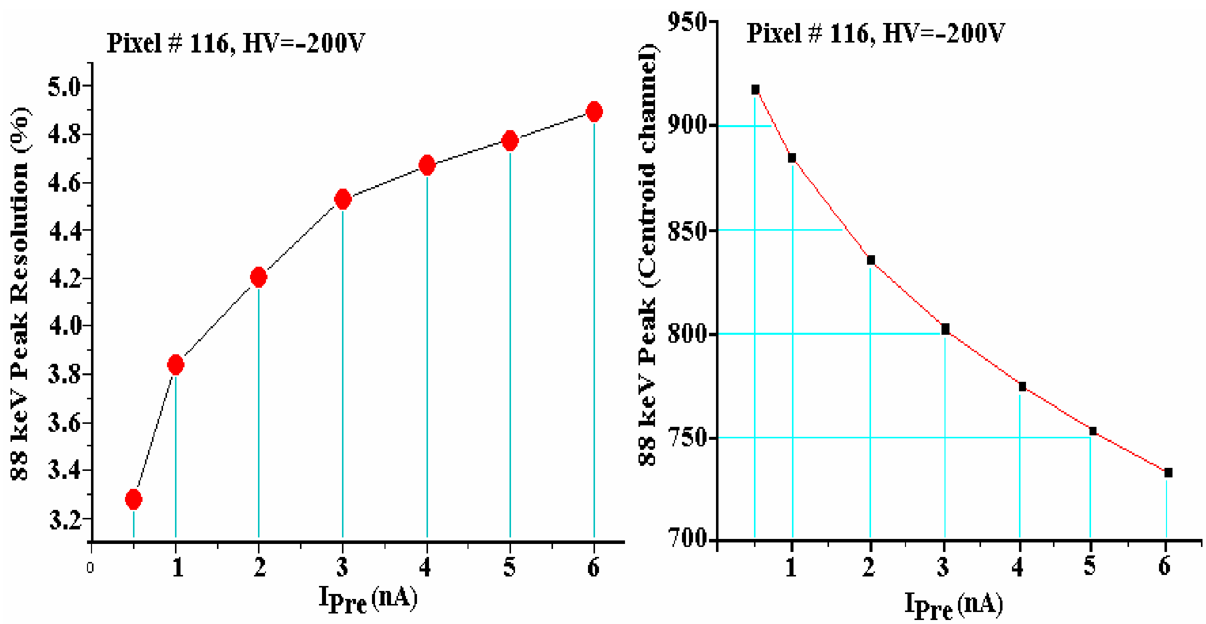

Fig. 5. ^{109}Cd 88 keV peak relative resolution (FWHM, left) and peak centroid variation (right) as a function of the bias current of the preamplifier 1st stage, I_{Pre}.

The drawbacks in the performance improvements (mainly noise) due to reductions of I_{Pre} are the following:

- the on-board ASIC-PCB potentiometer does not permit fine adjustements below 0.5 nA;
- values of I_{Pre} below 0.4 nA tend to reduce the dynamic range, i.e. X-ray energies higher than 80 keV tend to saturate;
- the first stage preamplifier tends to be unstable.

All the above reasons suggested to operate at $I_{Pre} \cong 0.5$ nA, which also gave satisfactory results with the pixel # 116; the same I_{Pre} value has been set in the ASIC PCB “C”.

The overall linearity (ASIC “A” response Vs input X-Ray energy) has been tested on pixel # 116 at $I_{Pre} \cong 0.5$ nA (data in Table II).

Table II. Linearity test data; pixel #116; ASIC PCB “A”.

Energy (keV)	Peak (Centroid)	Filename	Resolution (%)	ROI algorithm
22-24 (^{109}Cd)	258.36	CdA8 (3600 sec)	15.8	2nd deg
			14.3	4th deg
60 (^{241}Am)	645.31	AmB2 (14400 s)	5.0	2nd deg
			3.3	4th deg
88 (^{109}Cd)	916.57	CdA8 (3600 sec)	3.7	3rd deg
			3.8	4th deg

Fig. 6 shows the data extracted from Table II relative to $I_{Pre} \cong 0.5$ nA. An ^{241}Am source has been used to have the possibility to consider also the 59.5 keV X-Ray energy. The equation of the linearity straight line is:

Ch # $\cong$ 9.688 (Ch/keV)·E(keV) + 31.91 for pixel # 116 @ $I_{Pre} \cong 0.5$ nA

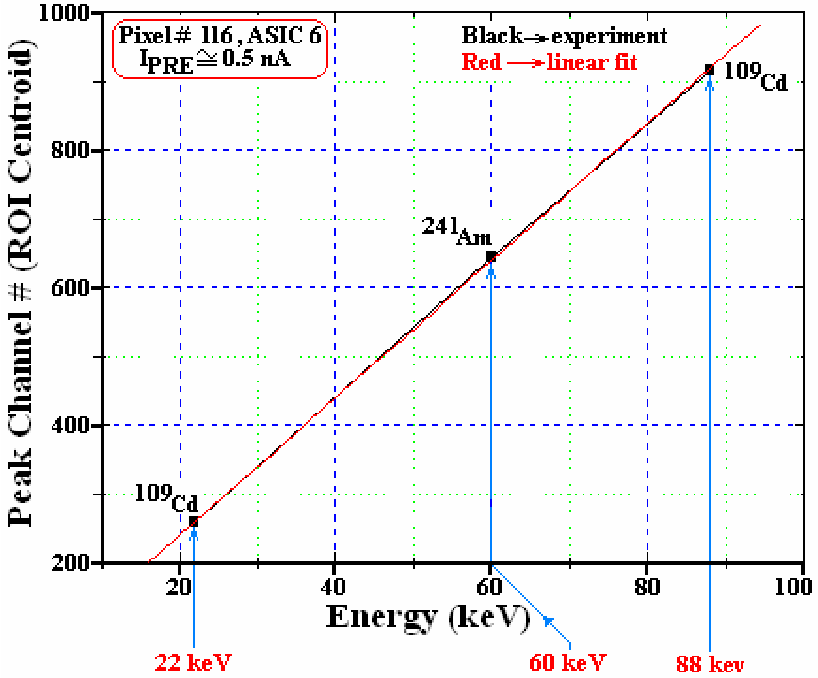

Fig. 6. Linearity response of the detection system to three different X-Ray energies.

From the stored spectra (^{109}Cd and ^{241}Am) the noise peak at low energies seems to involve channel not higher than 160, which means that the intrinsic ASIC+CZT overall noise is equivalent to 10-12 keV.

4. Tests on the channels of three ASIC PCBs.

4.1. Channel-to-channel non-uniformity test: semi-quantitative evaluation.

The output data organization of ASIC PCB "A", PCB "C" and PCB "D", connected to the detector I/O pad as told in § 2 and also shown in [Hybrid Exp-1], is listed in Table III.

Table III. ASIC PCBs logistics and data organisation

ASIC PCB "A"			ASIC PCB "C"			ASIC PCB "D"		
Filename	**ASIC**	**Ch #**	**Filename**	**ASIC**	**Ch #**	**Filename**	**ASIC**	**Ch #**
No file	6	1 unusable	Cd11	1	1 unusable	DCd61	6	1
Cd62	6	2	No file	1	2 unusable	DCd62	6	2
Cd63	6	3	Cd13	1	3 unusable	DCd63	6	3
Cd64	6	4	Cd14	1	4	DCd64	6	4
Cd65	6	5	Cd15	1	5	DCd65	6	5
Cd66	6	6	Cd16	1	6	DCd66	6	6
Cd67	6	7	Cd17	1	7	DCd67	6	7
No file	6	8 unusable	Cd18	1	8	DCd68	6	8

Any ASIC OUTPUT channel has been fed at a time to the same analog conditioning external equipment (see Fig. 4) and then converted and stored in the MCPHA. The X-Ray source used to irradiate the CZT detector is ^{109}Cd which surely does not saturate the amplification chain at the 22-26 peak energy. In fact, due to the external amplifier gain of 3.5 (Fig. 4), for some channels the 88 keV signal saturates and it is not usable for the computations. Otherwise the ^{241}Am source would require storing times too long and then impracticable for so many measurements. Then the evaluation of the channel-to-channel non-uniformity is based on the data relative to the 22-26 keV ^{109}Cd peak. Measurement data relative to ASIC PCB "A", "C", "D" are listed in Tables IV, V, and VI respectively. Channels labelled as "unusable" are too noisy, or they do not amplify and correctly shape the signal, or they are totally dead.

Table IV.

ASIC PCB "A". Position 6. Filename CdA6i						
Ch #	**Centroid 22-26 keV**	**Counts at 22-26 keV peak**	**Integral counts at 22-26 peak**	**Peak Noise Ch**	**Counts at noise peak**	**Integral noise count**
1	unusable	-	-	-	-	-
2	234.64	13414	748144	84	52183	1133468
3	232.64	23569	1171816	84	20508	506967
4	250.48	38218	1947583	84	21379	714766
5	272.75	17192	985051	82	39087	769532
6	268.82	21945	1382845	82	75982	1456182
7	238.67	17290	1231025	82	208204	3636487
8	unusable	-	-	-	-	-

Table V.

ASIC PCB "C". Position 1. Filename CdA1i						
Ch #	**Centroid 22-26 keV**	**Counts at 22-26 keV peak**	**Integral counts at 22-26 peak**	**Peak Noise Ch**	**Counts at noise peak**	**Integral noise count**
1	unusable	-	-	-	-	-
2	unusable	-	-	-	-	-
3	unusable	-	-	-	-	-
4	258.08	21949	1322637	84	20512	577603
5	260.54	24734	1253153	85	23500	641866
6	242.97	33101	1588130	84	17690	464514
7	258.23	14428	329965	82-83	47102	984189
8	251.51	23110	1569892	81-82	94055	1541019

Table VI.

ASIC PCB "D". Position 6. Filename DCd6i						
Ch #	**Centroid 22-26 keV**	**Counts at 22-26 keV peak**	**Integral counts at 22-26 peak**	**Peak Noise Ch**	**Counts at noise peak**	**Integral noise count**
1	172.11	28775	1138908	84	14744	419868
2	245.21	18019	926404	84	20530	450682
3	238.99	27111	1290496	85	19856	476312
4	246.83	52921	2425924	85	16384	318957
5	282.73	21192	1156963	84	25036	575234

6	262.24	27400	1390484	84	19625	461385
7	259.43	18258	1032676	83	38261	635690
8	217.56	23041	1070772	85	17227	473817

Ch #1 ASIC PCB "D" not well shaped and noisy; 88keV peak saturates for Ch #5, #7.
ROI background straight line or least square fit (1^{st} degree) for data in Tables from IV to VI.

To evaluate the channel-to-channel non-uniformity, for any measurement it was evaluated the mean centroid value given by the Aptek SW when considering the 22-26 keV peak ROI. The channel-to-channel non-uniformity has been calculated with the following relationship:

$$\delta_i = [<C> - C_i]/<C>$$

where:

$<C>$ = mean Centroid value calculated over 18 working channels = $[\Sigma_i\, C_i]/18 \cong 251.24$
Ci = centroid value calculated for the i-th channel
δ_i = deviation = measure of gain non-uniformity
The data used for the calculations of δ_i of the usable ASIC channels are listed in Table VII and represented in the hystogram of Fig. 7a.

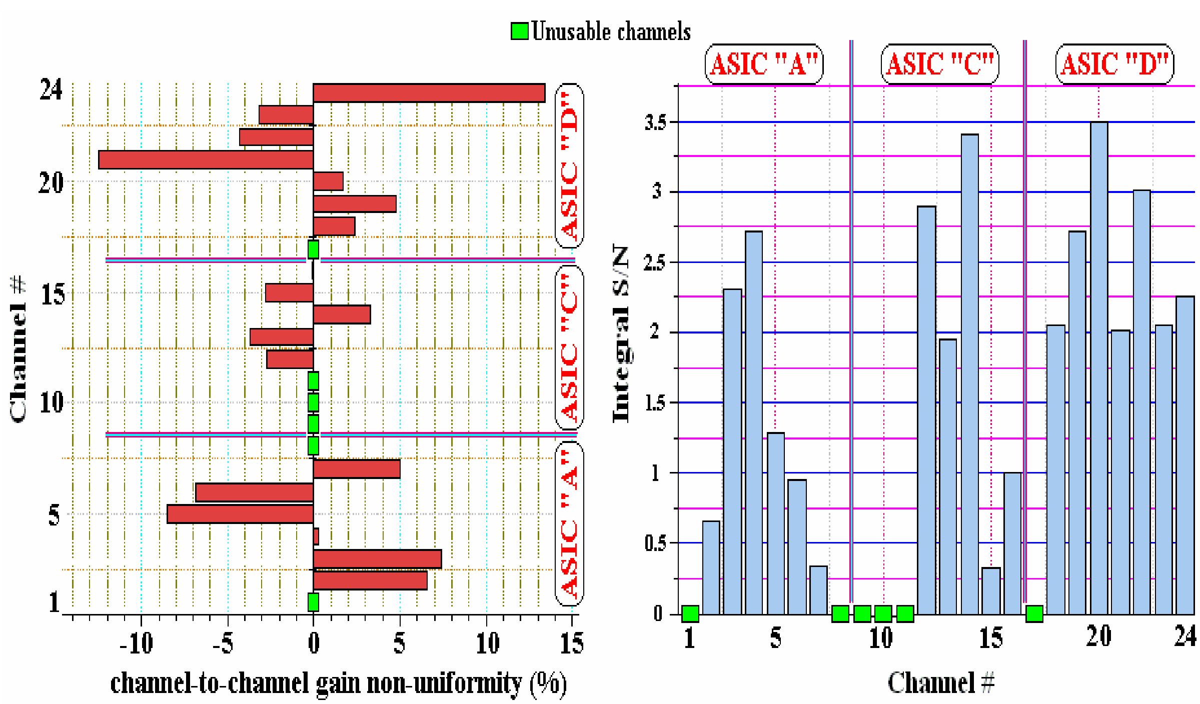

Fig. 7. Channel-to-channel non-uniformity, i.e. gain non-uniformity (histogram on the left: 7a). Estimated integral S/N ratio for the usable ASIC channels (histogram on the right: 7b).

Table VII. ASICs' channel gain non-uniformity

ASIC PCB "A"		ASIC PCB "C"		ASIC PCB "D"	
Channel	**δ_i (%)**	**Channel**	**δ_i (%)**	**Channel**	**δ_i (%)**
1	-	1	-	1	-
2	+6.6	2	-	2	2.4
3	+7.4	3	-	3	4.8
4	+0.3	4	-2.7	4	1.7
5	-8.5	5	-3.7	5	-12.5
6	-6.9	6	+3.3	6	-4.3
7	+5.0	7	-2.8	7	-3.2
8	-	8	-0.1	8	13.4

4.2. ASIC channels' S/N ratio test: semi-quantitative estimate.

In Table IV, V and VI for any usable channel are also listed evaluations (given as outputs of the Aptek analysis SW) of the integral counts under the 22-26 keV peak and the noise peak at lower energies. These data were used to have a very approximate idea of the S/N ratio of any ASIC channel. S/N data are listed in Table VIII and represented the histogram of Fig. 7b.

Table VIII. Data for the evaluation of the SNR for the ASIC channels

	ASIC PCB "A"			ASIC PCB "C"			ASIC PCB "D"		
Ch #	**S**	**N**	**Integral S/N**	**S**	**N**	**Integral S/N**	**S**	**N**	**Integral S/N**
1	-	-	-	-	-	-	-	-	-
2	748144	1133468	0.66	-	-	-	926404	450682	2.05
3	1171816	506967	2.31	-	-	-	1290496	476312	2.71
4	1947583	714766	2.72	1322637	577603	2.90	2425924	318957	3.5-6
5	985051	769532	1.28	1253153	641866	1.95	1156963	575234	2.01
6	1382845	1456182	0.95	1588130	464514	3.41	1390484	461385	3.01
7	1231025	3636487	0.34	329965	984189	0.33	1032676	635690	2.05
8	-	-	-	1569892	1541019	1.01	1070772	473817	2,26

5. Additional tests with ASIC PCB "D" in position 7.

As anticipated in § 2, the ASIC PCB "D" has also been placed in position 7 of the CZT detector output pad [Hybrid Exp1 and Fig. 19] in order to read out the pixels 179, 164, 148, 133, 118, 115, 120, 65.

In this configuration data were accumulated with the same procedure described in § 4. Data extracted from the measurements are given in Appendix II.

6. Spectroscopy tests on two ASIC channels.

Based on the S/N evaluation given above (Table VIII and Fig. 7b), the ASIC PCB "A" channel showing acceptable noise performance is the ch # 6, corresponding to the CZT pixel # 116, while for ASIC PCB "C" the best S/N ratio is found for ch # 6, corresponding to the CZT pixel # 134.

The three ASIC PCBs "A", "C", "D" operated at $I_{Pre} \cong 0.5$ nA. The signals from these ASICs' channels not saturating at the higher energy, i.e. 88 keV, have been separately processed with the set-up of Fig. 4 and data accumulated in MCPHA to have significative spectroscopic information.

The radioactive sources used for both the channels connected to the pixels # 116 (ASIC PCB "A") and # 134 (ASIC PCB "C") are ^{109}Cd (1800 or 3600 sec accumulation time) and ^{241}Am (28800 sec or 14400 sec accumulation times). Collected data (MCA histograms), which also could be used to re-verify the individual channel linearity, are presented in Figures from 9 to 14.

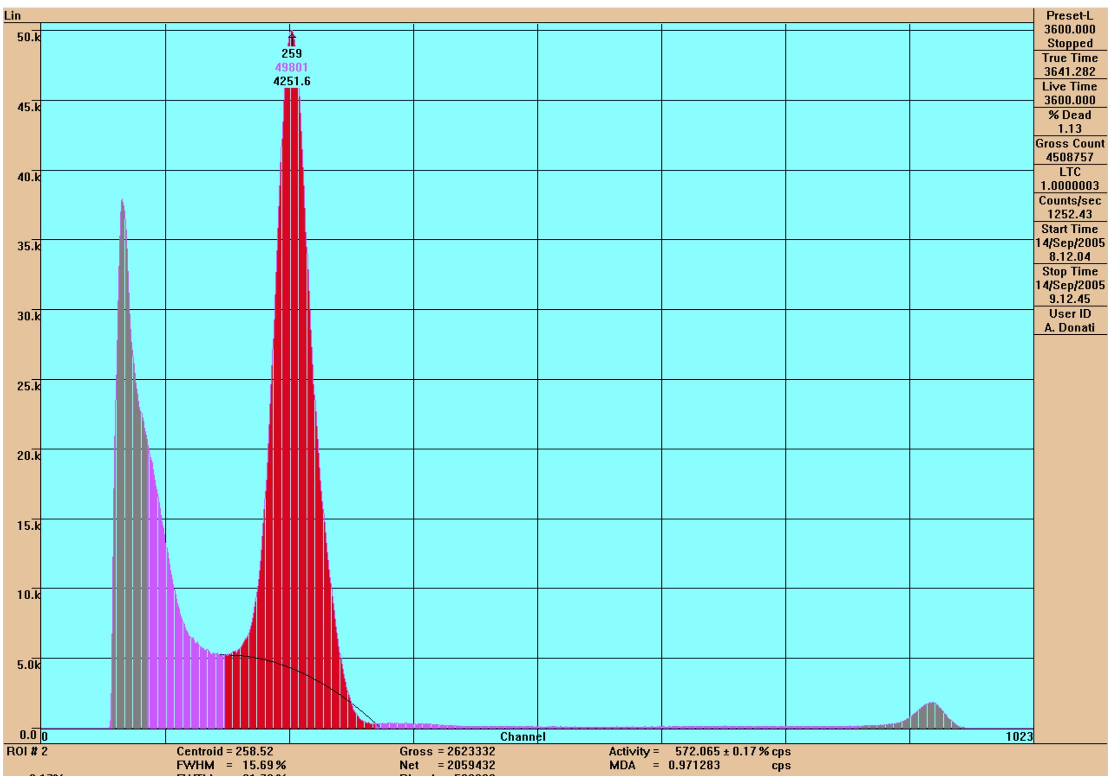

Fig. 9. Pixel # 116 spectra when irradiated with ^{109}Cd source. $I_{Pre} \cong 0.5$ nA. ROI properties: 2nd deg fit. 22-26 keV peak in evidence.

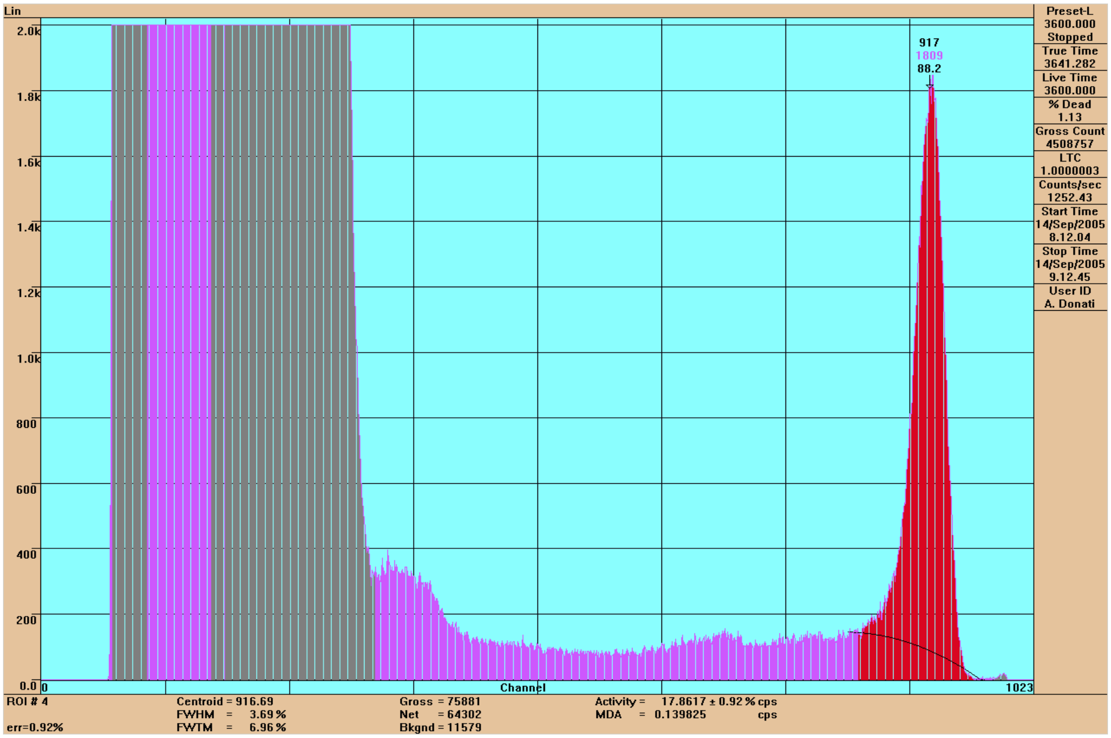

Fig. 10. Data as for Fig. 9 with the 88 keV peak expanded.

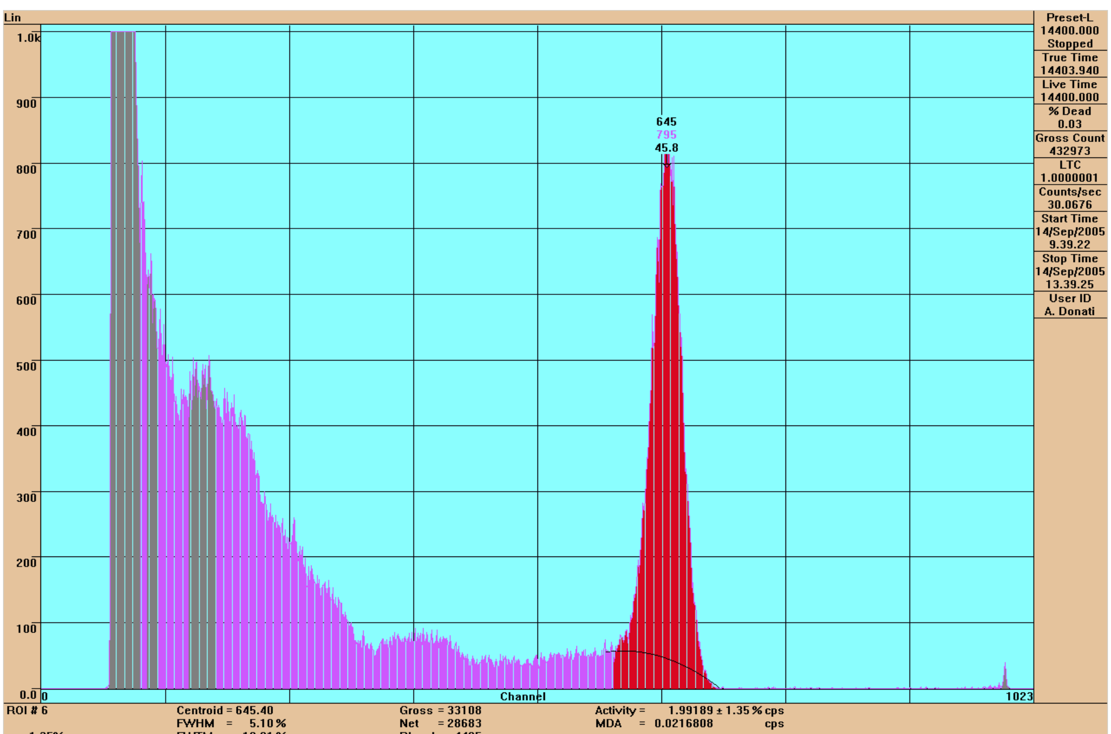

Fig. 11. Pixel # 116 spectra when irradiated with ^{241}Am source. $I_{Pre} \cong 0.5$ nA. ROI properties: 2nd deg fit. 59.5 keV peak in evidence.

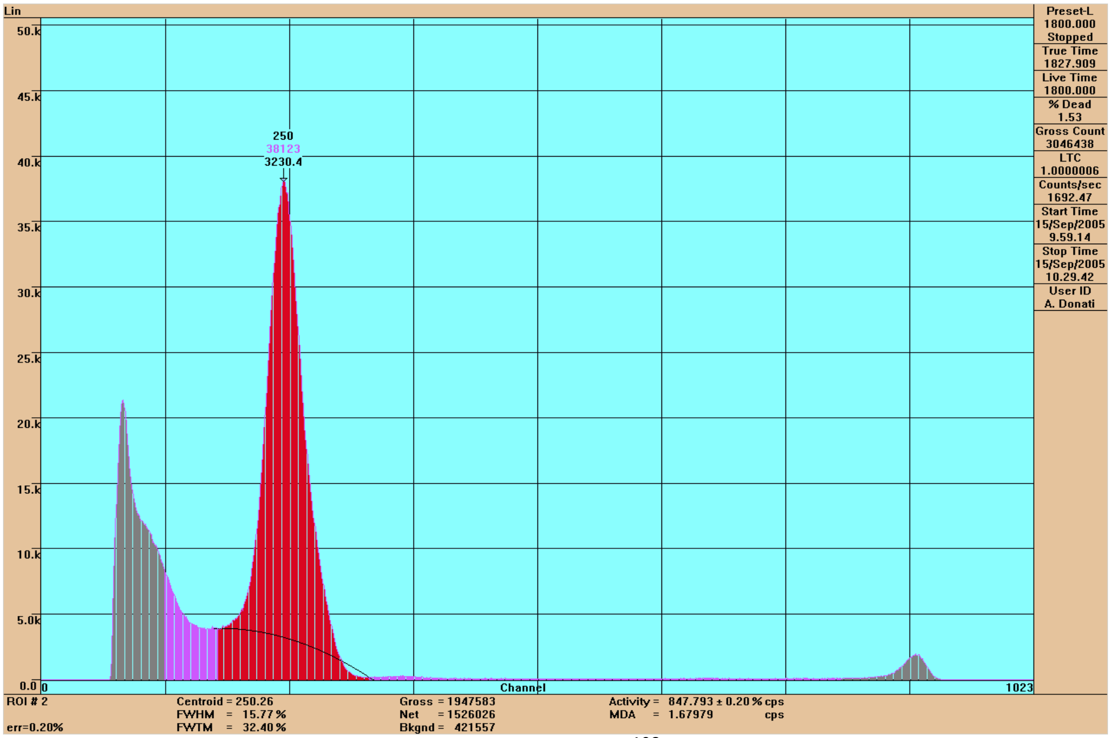

Fig. 12. Pixel # 134 spectra when irradiated with ^{109}Cd source. $I_{Pre} \cong 0.5$ nA. ROI properties: 2nd deg fit. 22-26 keV peak in evidence.

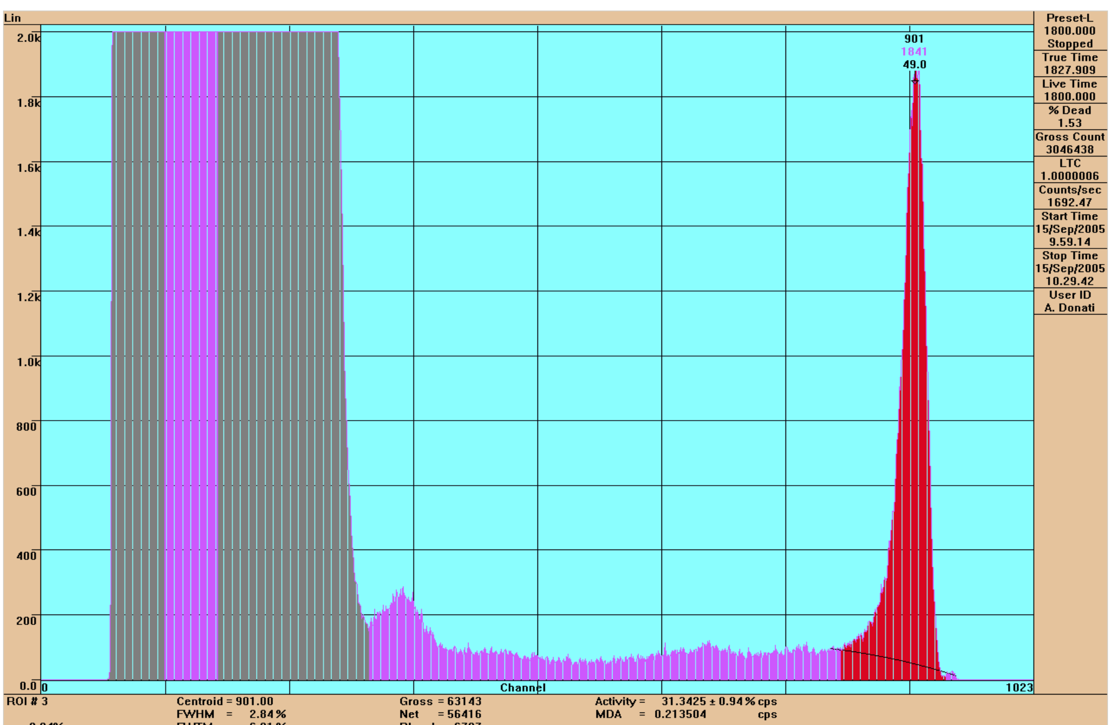

Fig. 13. Data as for Fig. 12 with the 88 keV peak expanded but near saturation.

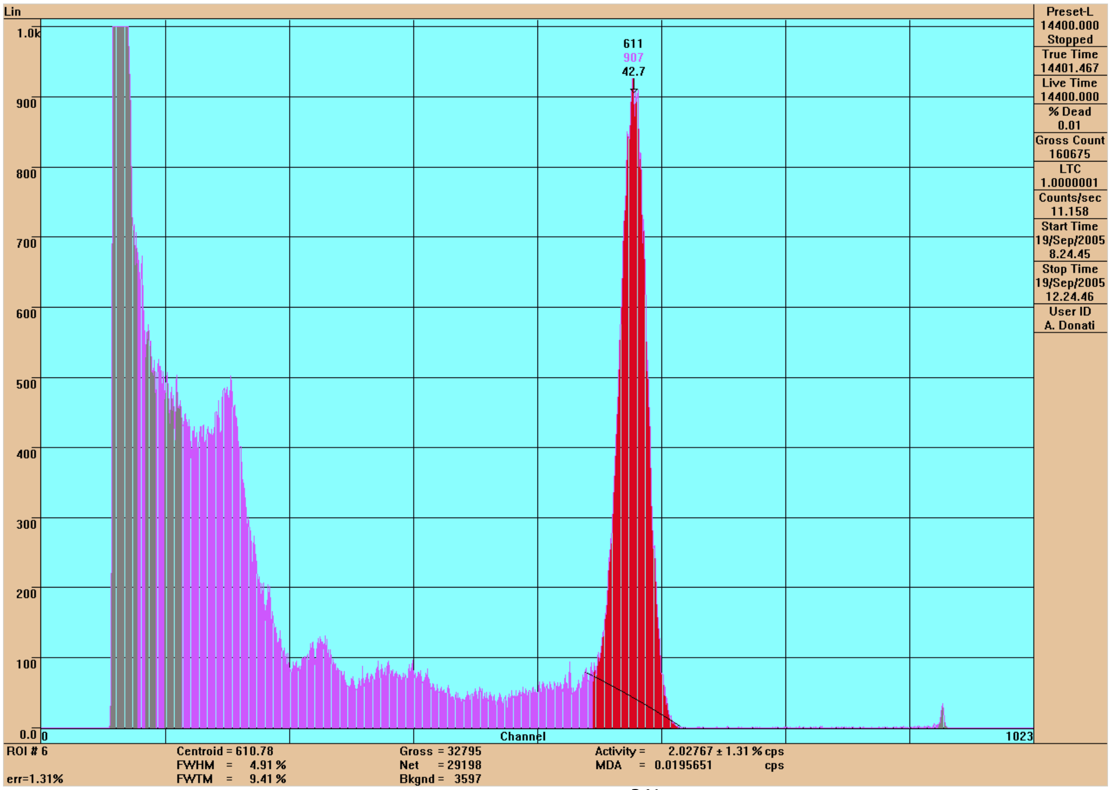

Fig. 14. Pixel # 134 spectra when irradiated with ^{241}Am source. $I_{Pre} \cong 0.5$ nA. ROI properties: 2nd deg fit. 59.5 keV peak in evidence.

7. Evaluation of the energy resolution of the tested ASICs' channels.

By considering the collected data relative to both ^{241}Am and ^{109}Cd sources, an approximate evaluation of the energy resolution (FWHM) can be given for the tested ASICs' channels. The Fig. 15 reports the energy resolutions of the estimated best and worst ASICs' channels: any other ASICs' channel tested should have an energy resolution behaviour intermediate between the upper and the lower curve.

It has to be noted that the estimated energy resolution is not that intrinsic relative to the ASIC channel considered,

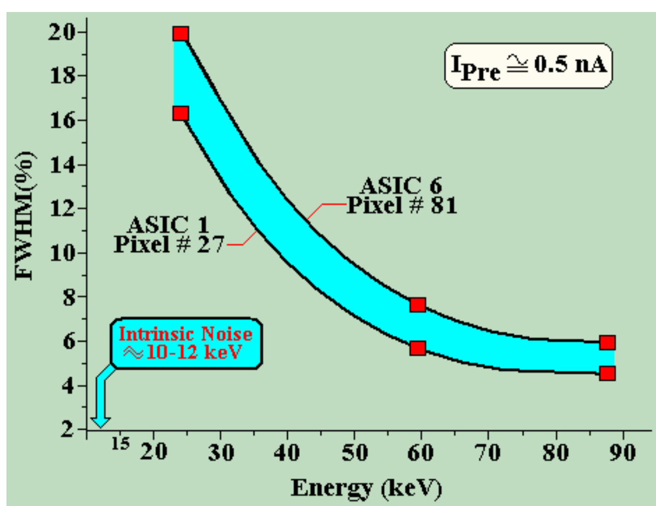

Fig. 15. Semi-quantitative evaluation of the energy resolution of the ASIC tested channels. The upper curve represents the energy resolution of the channel connected to the pixel # 133, the lower one to the pixel #27: any other channel tested should have energy resolution comprised in the intermediate band.

but rather the result of the CZT pixel-ASIC channel combination, and then also including the noise contribution (parallel and series noise) of the detector element. The Fig. 16 shows the spectra accumulated after processing the signal from the CZT pixel # 116 with the channel 6 of the ASIC PCB “D”. Since the same pixel has been processed also by the ASIC PCB “A” (Fig. 11), the two spectra can be compared to have an idea of the response of different ASIC connected to the same CZT detector element.

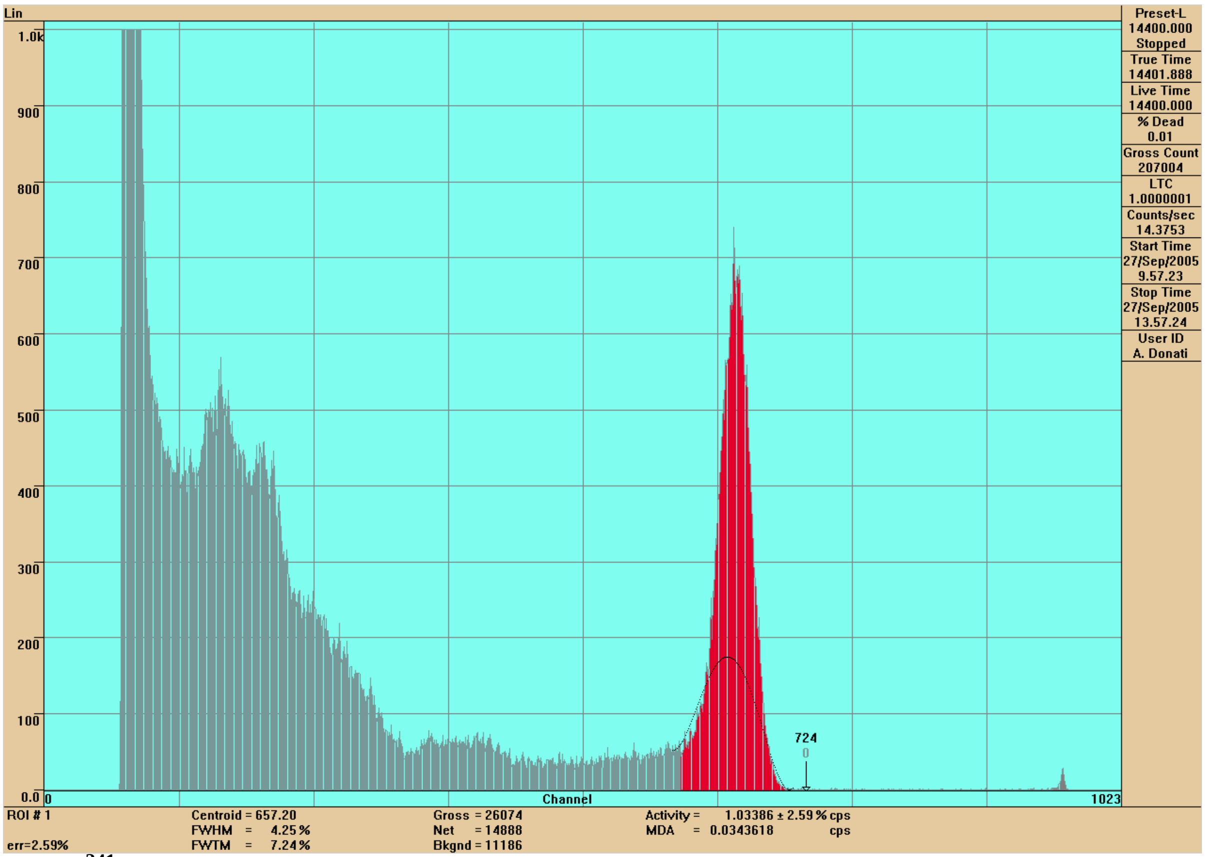

Fig. 16. **^{241}Am spectra accumulated with channel # 6 of ASIC PCB “D” connected in position 6 of the CZT output pad. Pixel # 116, $I_{Pre} \cong 0.5$ nA. ROI properties: 4th deg fit; 59.5 keV peak in evidence. Data can be compared with those shown in Fig. 11.**

8. The CZT+ASIC seen by the acquisition equipment for Leicester Hybrid Tests.

In preparation of the combined experiment Leicester-IASF(Bo-Pa) the available ASIC "A" and "C" PCBs channels have been connected to a 16 channels Multiparametric Electronics (Takes); this set-up is similar to the experiment arrangement that will be used to read out an homogeneous subset of CZT detector pixels using 14 ASIC PCB connected with the CZT pixel detector in the tests at the Leicester University [Hybrid Exp1].

The 16 ASIC output channel are sent to the 37 pin input connector of the Takes electronics through a couple of multiple cables each of which is protected with an external copper shield. Any multiple 1.5 meter cable transfers 8 signals to Takes electronics, so serving an 8-chs ASIC PCB. Because the large internal gain set for any channel in the Takes Electronics (~50), the signals from the ASICs' channels would saturate. This dictates a reduction in gain which was implemented by inserting (in series) on any ASIC output channel a 27 kOhm resistor.

Using this processing and acquisition system we have performed a series of quick and short tests with a ^{109}Cd un-collimated source with the aim to check the functionality of the entire detection chain. In the following figures are shown some shots of the LABIEW quick-look screen taken during the acquisition. Because the two ASIC PCB channels have been connected to the Takes input from 0 to 15, the quick look software show the data as read from an array of 4x4 pixel.

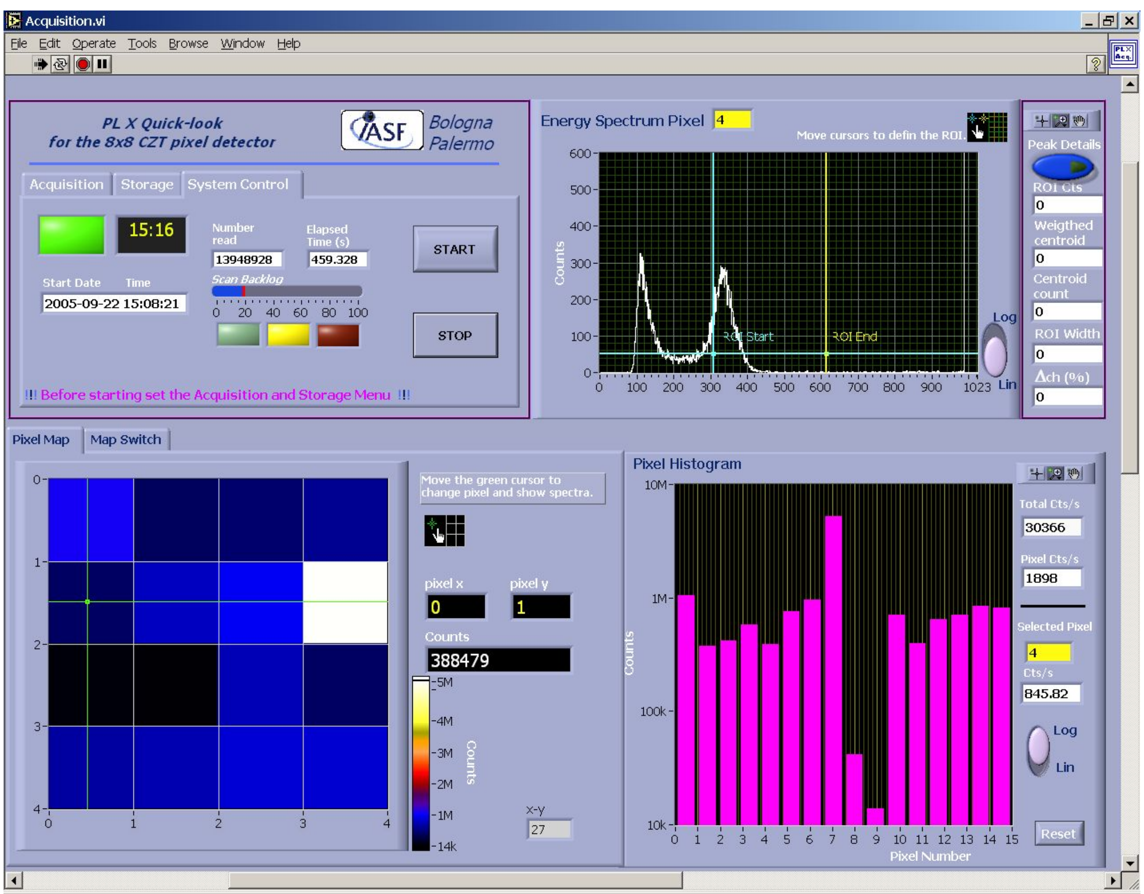

Fig. 17. The LABVIEW quick-look screen. In the left bottom the false color map of the 16 ASIC's channel counts seen as an array of 4x4 contiguous pixels; in the top right window the spectrum from the ASIC "A", channel 4 (corresponding to CZT pixel # 134); in the bottom right the histogram of the channel counts.

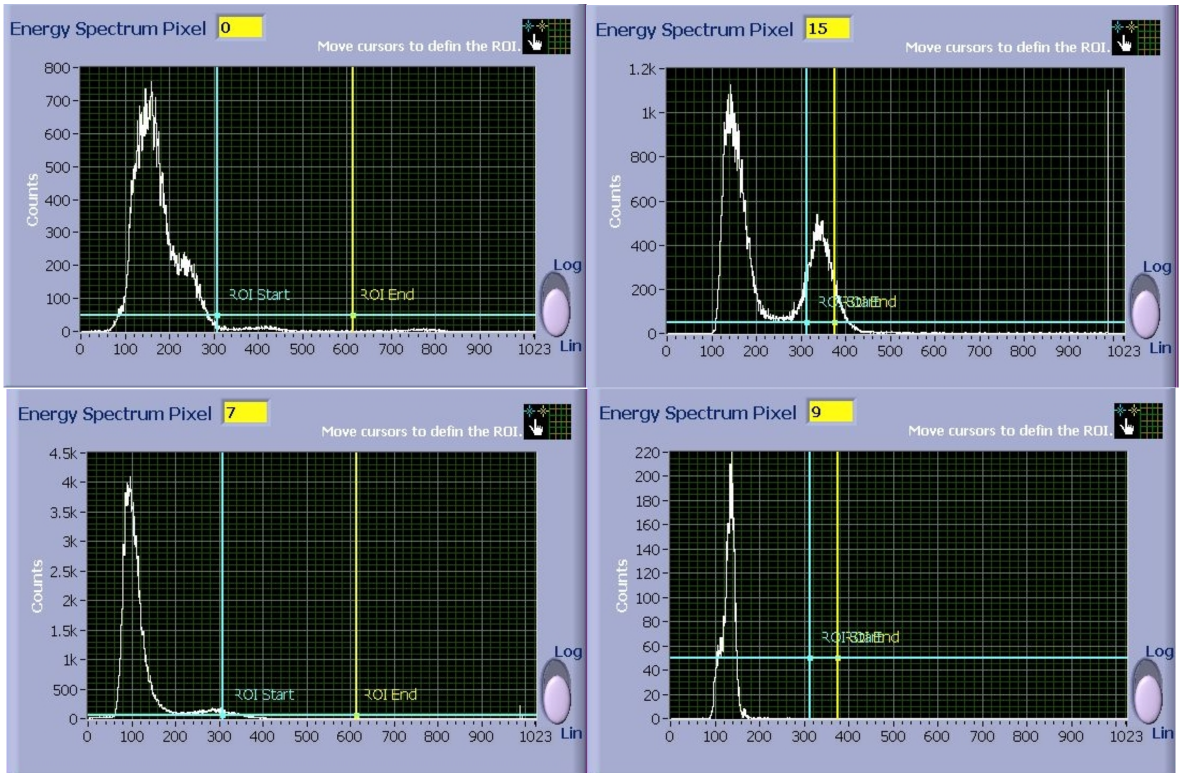

Fig. 18. Some ^{109}Cd obtained from a sample of the ASIC channels with the complete processing and acquisition chain. (top left) Spectrum of the ASIC "A" channel 6: the gain of this channel allow to see both low and high energy lines of the source; (top right) a high gain ASIC channel in which are well visible the 22/26 keV peak but the 88 keV is out of scale as demonstrated by the one channel line at the end of the channels scale; (bottom left); a high noise ASIC channel that show a very large noise count rate (lower channel peak) with respect to the 22/26 keV one; (bottom right) a 'dead' ASIC channel.

The counts map and histogram in Fig. 17 show clearly the uniformity of the CZT+ASIC channel response as well as the noisy pixels/channels (white) and the dead ones (black). In the Fig. 18 shots of the spectra obtained during the test are shown for an indicative sample of ASIC channels. The first two (top) shots are from good ASIC channels showing a different gain, while the second row of spectra (bottom) show the behaviour of a noisy channel and a almost dead one.

9. Conclusions.

As often told in the report, the main goal of the activity was to test the whole detection equipment, i.e. a subset of the CZT detector pixels combined with the available front-end active devices (ASICs). In fact, it was not possible to fully characterize the 2nd version of the ASIC from a pure electrical point of view owing to two drawbacks due to both the design and fabrication.

The first one, which has a strong impact on the usable ASIC channels and ASIC PCBs, depends on the fact that on the ASIC die the input pad tracks were undersized and too thin, which caused a number of failures during the deposition of the bondings connecting the ASIC input channels to the ASIC PCB input connector. This shortcoming has produced a mortality of the ASIC channels or whole ASICs which were not possible to recover.

The second one is similar to the first and refers to the test input pads; again, during the bonding to the external and probably due to the excessive proximity of the electrical tracks on the ASIC die, during the bonding deposition the electrical connection was unreliable.

As a result, it was not possible to electrically test the individual ASIC channels.

The outputs of the tests performed and reported above seem to confirm that there is a remarkable mortality caused by the bonding process of the ASIC inputs to the external world (detector and test): three ASIC PCBs over five available were usable, and 18 channels over 24 were working. Surely it is not possible to state that there is a signicative statistics (maybe at least 10 ASIC PCBs should be tested) to provide an evaluation of the mortality. What seems to be reasonable is that the tests have more a sampling feature and it is quite probable that the faults have been produced during the bonding process. The usable channels (18 testable over 24) of the operative ASIC PCBs have been found to work within the expected performances which does not seems to discourage to program the use the ASIC in future applications, provided that the ASIC design and fabrication be able to overcome the above defects.

10. Appendix I: list of the measurements.

Filename	I_{Pre} (nA)	Pixel #	Live Time (sec)	Notes
CdA1	6.1	116	21600	Collimated source ϕ=1.5 mm
CdA2	6.1	116	3600	Collimated source ϕ= 3 mm
CdA3	5.1	116	3600	Collimated source ϕ= 3 mm
CdA4	4.1	116	3600	Collimated source ϕ= 3 mm
CdA5	3.1	116	3600	Collimated source ϕ= 3 mm
CdA6	2.1	116	3600	Collimated source ϕ= 3 mm
CdA7	1.0	116	3600	Collimated source ϕ= 3 mm
CdA8	0.52	116	3600	Collimated source ϕ= 3 mm
CdA11	0.52	70	3600	Collimated source ϕ= 3 mm
CdA13	0.52	104	3600	Collimated source ϕ= 3 mm
CdA14	0.52	105	3600	Collimated source ϕ= 3 mm
CdA15	0.52	73	3600	Collimated source ϕ= 3 mm
CdA16	0.52	27	3600	Collimated source ϕ= 3 mm
CdA17	0.52	90	3600	Collimated source ϕ= 3 mm
CdA18	0.52	91	3600	Collimated source ϕ= 3 mm
CdA62	0.52	178	3600	Collimated source ϕ= 3 mm
CdA63	0.52	161	3600	Collimated source ϕ= 3 mm
CdA64	0.52	134	3600	Collimated source ϕ= 3 mm
CdA65	0.52	132	3600	Collimated source ϕ= 3 mm
CdA66	0.52	116	3600	Collimated source ϕ= 3 mm
CdA67	0.52	81	3600	Collimated source ϕ= 3 mm
DCd61	0.52	194	3600	Collimated source ϕ= 3 mm
DCd62	0.52	178	3600	Collimated source ϕ= 3 mm
DCd63	0.52	161	3600	Collimated source ϕ= 3 mm
DCd64	0.52	134	3600	Collimated source ϕ= 3 mm
DCd65	0.52	132	3600	Collimated source ϕ= 3 mm
DCd66	0.52	116	3600	Collimated source ϕ= 3 mm
DCd67	0.52	81	3600	Collimated source ϕ= 3 mm
DCd68	0.52	66	3600	Collimated source ϕ= 3 mm
DCd71	0.52	179	3600	Collimated source ϕ= 3 mm
DCd72	0.52	164	3600	Collimated source ϕ= 3 mm
DCd73	0.52	148	3600	Collimated source ϕ= 3 mm
DCd74	0.52	133	3600	Collimated source ϕ= 3 mm
DCd75	0.52	118	3600	Collimated source ϕ= 3 mm
DCd76	0.52	115	3600	Collimated source ϕ= 3 mm
DCd77	0.52	120	3600	Collimated source ϕ= 3 mm
DCd78	0.52	65	3600	Collimated source ϕ= 3 mm
AmB1	1.0	116	28800	Collimated source ϕ= 3 mm
AmB2	0.52	116	14400	Collimated source ϕ= 3 mm
AmC1	0.52	134	28800	Collimated source ϕ= 3 mm
Am16	0.52	27	14400	Collimated source ϕ= 3 mm
DAm66	0.52	116	14400	Collimated source ϕ= 3 mm

Measurements labeled "Cdxyz" performed with ^{109}Cd X-Ray source
Measurements labeled "Amqk" performed with ^{241}Am X-Ray source

The positionings of the three ASIC PCBs used in the tests is shown in Fig. 19, while the CZT pixels processed with the arrangement of Fig. 19 are shown in Fig. 20.

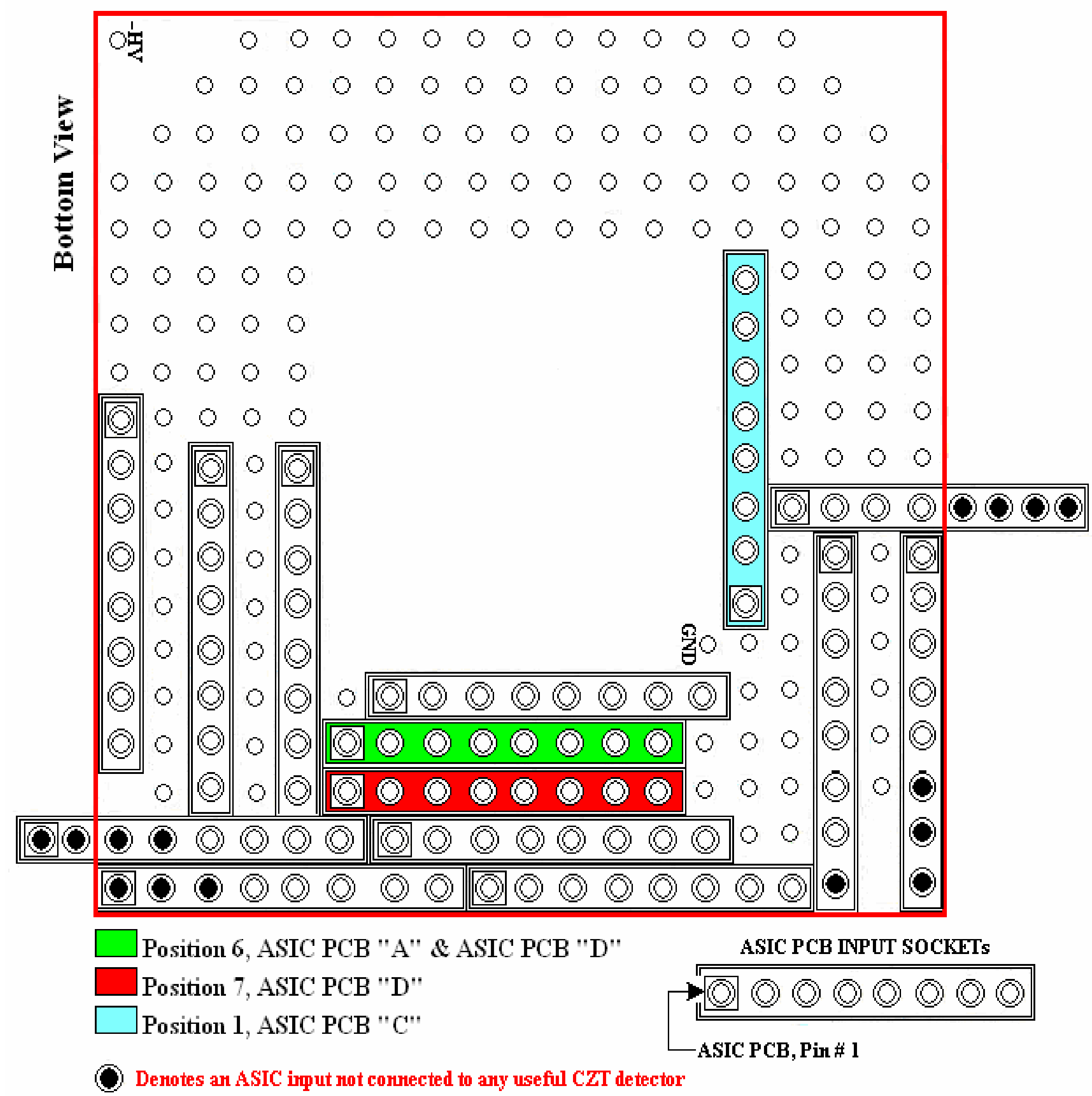

Fig. 19. ASIC PCBs positions in the tests. View from the CZT detector bottom (CZT detector I/O pad).

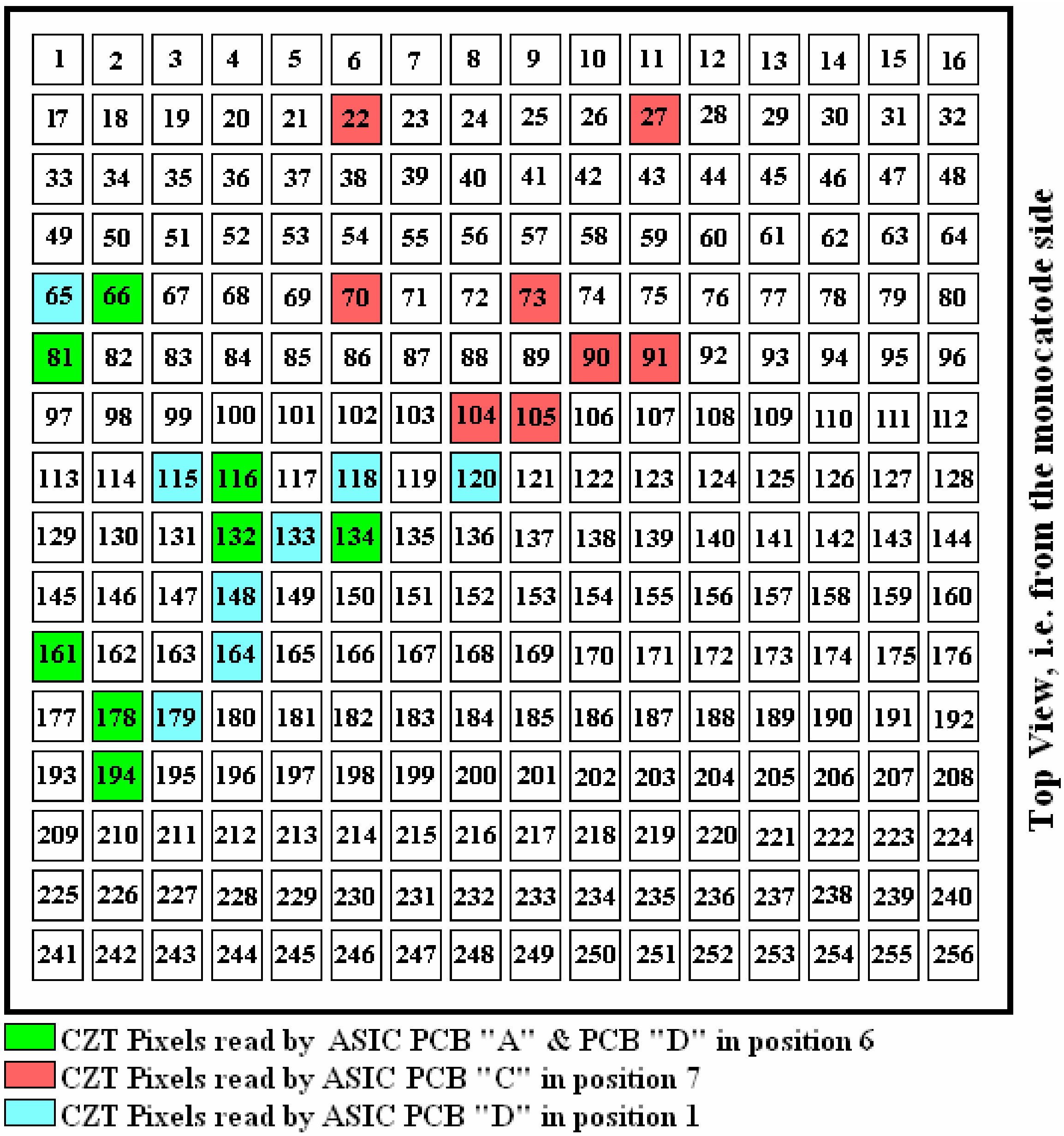

Fig. 20. CZT pixels tested over 256 available.

11. Appendix II: results of the tests performed with ASIC PCB "D" in position 7.

Data collected with ASIC PCB "D" in position 7 (Fig. 19) are summarized in Table IX and can be directly compared with the data processed by the same ASIC PCB placed in position 6 (Fig. 19). Since the same channel of the ASIC is used to alternately amplify the charge delivered by two separate CZT elements, the comparision between the data of the Tables IX and X can give an approximate evaluation of the influence of the CZT pixel, mainly due to the intrinsic capacity of the distinct detector elements. In particular, since the impulsive voltage $\mathbf{v(t)}$ induced by an X-Ray event in a detector pixel having a capacity $\mathbf{C}$ is approximately given by $\mathbf{v(t) \propto [1/C]\cdot\int i(t)\cdot dt}$, the quotient $\mathbf{V_{7i}}(22\text{keV})/\mathbf{V_{6i}}(22\text{keV})$ between the centroids of the same ASIC amplification channel, $\mathbf{i}$, connected to two different CZT pixels, should give an information on $\mathbf{C_{6i}/C_{7i}}$, i.e. on the ratio of the detector capacitances:

$$\mathbf{V_{7i}}(22\text{keV})/\mathbf{V_{6i}}(22\text{keV}) \propto \mathbf{C_{6i}/C_{7i}}$$

Table IX.

ASIC PCB "D". Position 7. Filename DCd7i

Ch #	CZT pixel #	Centroid 22-26 keV	FWHM (%)	Centroid 88 keV	FWHM (%)	Notes
1	179	-	-	-	-	
2	164	243.20	16.1	874.98	3.7	
3	148	253.87	15.1	918.90	3.4	
4	133	253.83	14.2	916.01	3.2	
5	118	281.90	14.0	-	-	**88 keV saturated**
6	115	264.76	15.3	933.58	2.5 (?)	**88 keV near saturation**
7	120	252.90	18.1	-	-	**88 keV saturated**
8	65	216.23	16.8	768.13	4.6	

Table X.

ASIC PCB "D" in position 6. Filename DCd6i.

Ch #	CZT pixel #	Centroid 22-26 keV	FWHM (%)	Centroid 88 keV	FWHM (%)	Notes
1	194	-	-	-	-	
2	178	245.21	14.1	876.22	3.6	
3	161	238.99	15.4	876.31	3.3	
4	134	246.83	13.8	905.00	3.4	
5	132	282.73	14.5	-	-	**88 keV saturated**
6	116	262.24	14.8	927.41	2.8 (?)	**88 keV near saturation**
7	81	259.43	16.1	-	-	**88 keV saturated**
8	66	217.56	16.6	767.07	3.5	

Capacitance ratio data are reported in Table XI and shown in Fig. 21. As it can be verified, the value of the capacitance of the pixel considered do not differ one from another by more of few %.

Table XI

Ch #	Postion 7 pixel	Postion 6 pixel	V_{7i}(22keV)/V_{6i}(22keV) $\propto$ C_{6i}/C_{7i}	Notes
1	179	194	-	Noisy ASIC channel
2	164	178	**0.992**	-
3	148	161	**1.062**	-
4	133	134	**1.028**	-
5	118	132	**0.997**	-
6	115	116	**1.009**	-
7	120	81	**0.978**	-
8	65	66	**1.001**	-

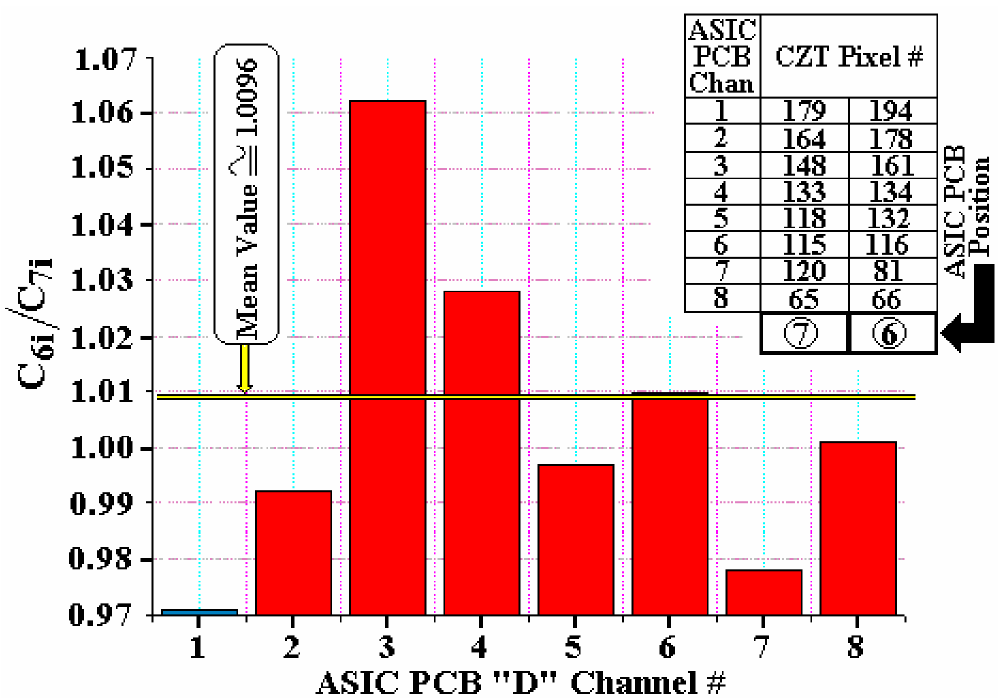

Fig. 21. Calculated capacitance ratio C_{6i}/C_{7i} for different pixels processed by the same ASIC PCB "D" successively placed in position 6 and 7.