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KEYWORDS

ICARUS **I**mager **C**harge **A**mplifier and **R**eado**u**t **S**ystem

SDC **S**ilicon **D**rift **C**hamber (also SDD)

SDD **S**ilicon **D**rift **D**etector

ASIC **A**pplication-**S**pecific **I**ntegrated **C**ircuit

MPW **M**ulti-**P**roject **W**afer integration

CSA **C**harge-**S**ensitive **A**mplifier

DAC **D**igital-to-**A**nalog **C**onverter

MSB **M**ost **S**ignificant **B**it

LSB **L**east **S**ignificant **B**it

RVS **R**educed **V**oltage **S**wing

CMDO **C**urrent-**M**ode **D**igital **O**utput

AFEE: **A**nalogue **F**ront **E**nd **E**lectronics.

DFEE: **D**igital **F**ront **E**nd **E**lectronics.

PD: **P**hoto**D**iode.

1. INTRODUCTION

1.1. Purpose and scope

Scope of this document is to report on the on the ICARUS-SDC ASIC, its interfaces with the external environment, the performance of the ASIC as well as the room for improvement for future devices.

1.2. Structure of the document

The document is structured as follow:

Chapter 2 gives a functional description of the device.
The chip is described within its external environment in chapter 3.
The ASIC outline and pin assignment are reported in chapter 4.
Chapter 5 describes circuit operation.
The ASIC operation test and performances are reported in chapter 6.
In chapter 7 is reported an example of ICARUS_SDC use.
Chapter 8 gives some hint on the use of the chip in space environment.
Possible further development are discussed in chapter 9 with the description of a new device.

1.3. Applicable documents

No documents are applicable in this specification.

2. FUNCTIONAL DESCRIPTION

The ICARUS-SDC ASIC is an integrated multichannel analogue front-end and read-out system.
The ASIC is in charge for the management of 16 PD signals form independent detectors. The design of the system has been optimised for its use with Silicon Drift Detector photodiodes operating either as direct low energy X-ray radiation detector or coupled to scintillator crystals for higher energies.

Fig. 1 shows the ASIC functional diagram. It includes 2 x 8 processing chains each of them composed of:

1) Charge preamplifier (with JFET externally mounted into the SDC)
2) Shaping amplifier (8 channels with 0.5 μsec shaping time, 8 channels with 3 μsec shaping time
3) Peak detector & Hold stage
4) Amplitude discriminator (trigger)

Moreover, the ASIC includes a 16 channel analogue multiplexer for pulse data sorting together with a sparse readout logic and a trigger logic.

After recording an event at its inputs the ASIC makes available the following data:

1) The input pulse(s) amplitude(s) data available at the ANALOG OUTPUT pin.
2) The input pulse precision time-mark given by the DATA_READY signal leading edge.
3) A four bits PIXEL_ADDRESS(0,3) bus , representing the channel(s) under read-out.

Channels without fired discriminator are skipped during readout (sparse readout logic).
Channels firing in coincidence with a VETO signals will not be sampled and analysed

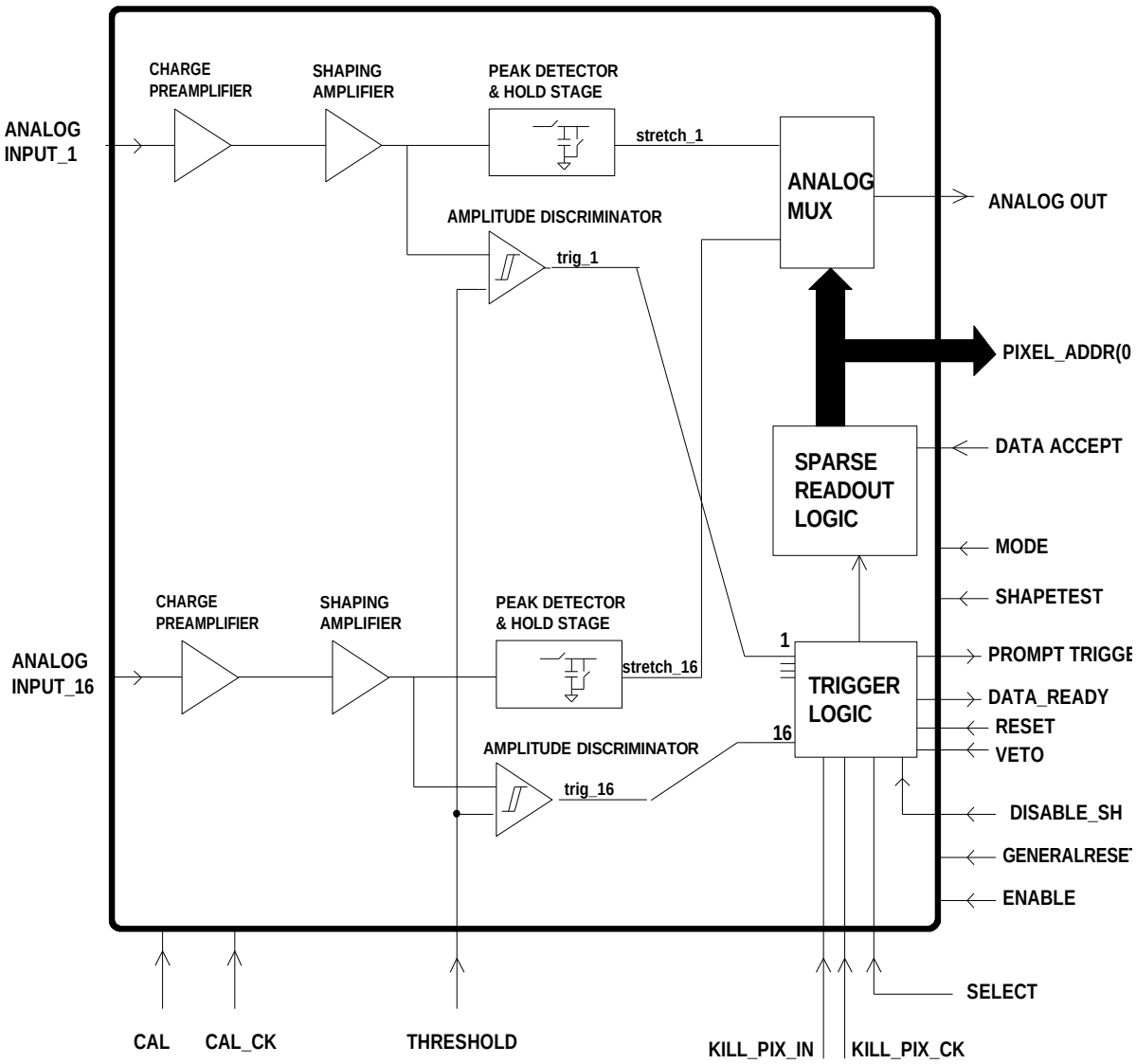

Fig. 1 ASIC FUNCTIONAL DIAGRAM

3. ICARUS-SDC CHIP INSIDE THE EXTERNAL ENVIRONMENT

In Fig. 2 the external environment of the ICARUS-SDC chip is depicted.

In the left most part of the figure the detector interface is shown while the right most side shows the interface with the processing chain.

The input stage of each channel is a simple voltage amplifier, followed by a semi-gaussian shaping amplifier.

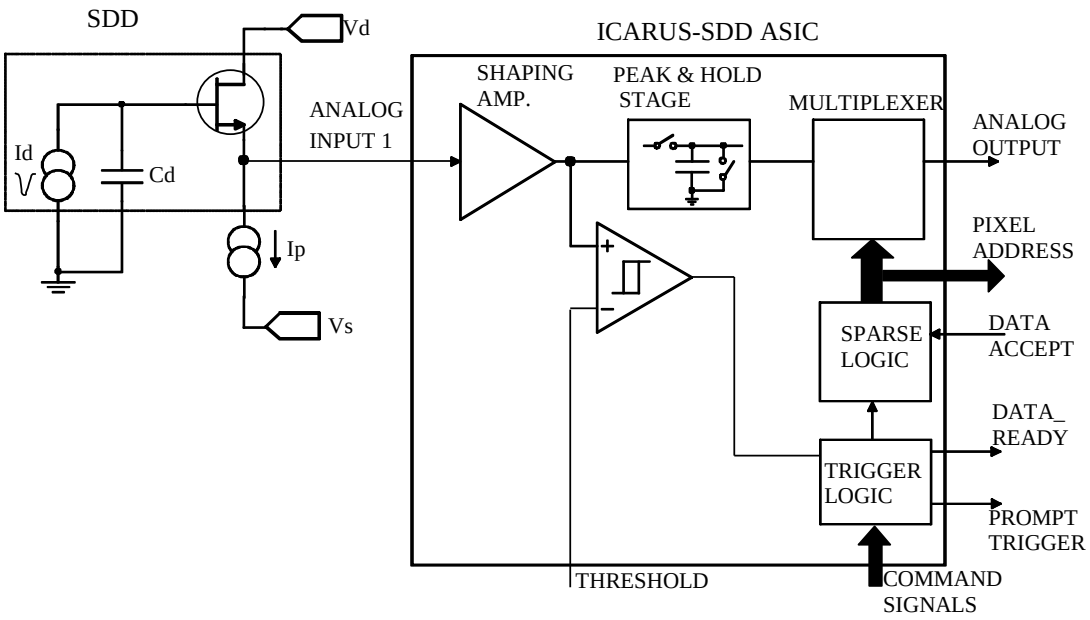

Fig. 2 ICARUS-SDC ASIC EXTERNAL ENVIRONMENT

4. ICARUS ASIC outline

The ASIC Pin assignment is shown in the Fig. 3 below.

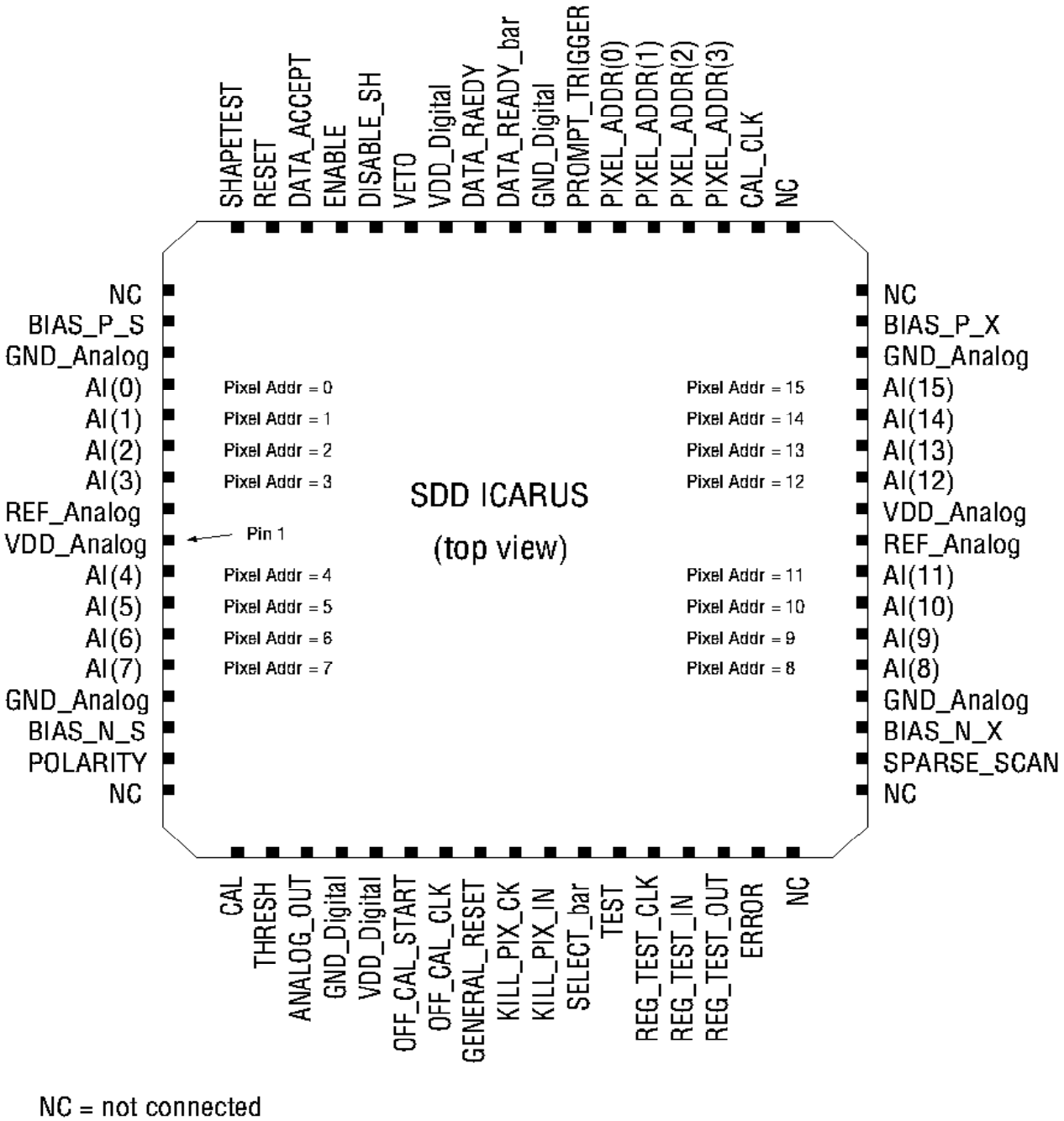

Fig. 3 ICARUS ASIC CLCC-68 package pin assignment.

4.1. Pin function and signal description

Pin name	Type	Signal class (note #)	Function
AI(0…7)	Input	Analog Voltage (1)	Analog inputs from external CSA (SDD)
AI(8…15)	Input	Analog Voltage (1)	Analog inputs from external CSA (X-ray)
BIAS_P_S	Passive	Analog Voltage (2)	Bias voltage check/decouple for chan. 0…7
BIAS_N_S	Passive	Analog Voltage (3)	Bias voltage check/decouple for chan. 0…7
BIAS_P_X	Passive	Analog Voltage (2)	Bias voltage check/decouple for chan. 8…15
BIAS_N_X	Passive	Analog Voltage (3)	Bias voltage check/decouple for chan. 8…15
POLARITY	Input	CMOS (Active HIGH) (4)	Polarity change for analog inputs AI(0…7)
SPARSE_SCAN	Input	CMOS (Active HIGH) (4)	Select sparse data scan (1, ICARUS standard) or full readout (0)
GENERAL_RESET	Input	CMOS (Active HIGH)	General Reset input for digital and all channel Peak & Hold circuits
RESET	Input	RVS (Active HIGH)	Input to reset Peak & Hold, trigger and related readout logic
VETO	Input	RVS (Active HIGH)	Inhibit data storage for veto coincident events
PROMPT_TRIGGER	Output	CMDO (Active SINK)	Time-stamp for each event exceeding the threshold, regardless of the veto status
DATA_READY	Output	CMOS (Active HIGH)	Flag to indicate the presence inside the ASIC of valid data to be read out
DATA_READY_bar	Output	CMOS (Active LOW)	
DISABLE_SH	Input	RVS (Active HIGH)	Input to prevent the ASIC from acquiring new events
ENABLE	Input	RVS (Active HIGH)	Enabling of the 3-state input/output to listen/talk on bus
DATA_ACCEPT	Input	RVS (Active HIGH)	Prompt for next data
PIXEL_ADDR(0…3)	Output	CMDO (Active SINK)	Current read out channel address
ANALOG_OUT	Output	0…500mV wrt. REF Analog Voltage Output	Buffered output voltage for the analog data
CAL	Bi-directional	Analog Voltage	Formerly calibration input (only used for internal threshold level measurement)
CAL_CLK	Input	CMOS (Active HIGH)	Clock for CAL shift register (for ShapeTest function)
THRESH	Input	Analog 0…2.5V	Threshold level
SHAPETEST	Input	CMOS (Active HIGH)	Input to disable the stretching function in order to observe the shaper output signal
OFF_CAL_START	Input	CMOS (Active HIGH)	Input to start the offset auto-calibration procedure
OFF_CAL_CK	Input	CMOS (Active HIGH)	Input to clock the offset auto-calibration procedure

Pin name	Type	Signal class	Function
REG_TEST_IN	Input	CMOS (Active HIGH) (4)	Input to the FIFO register with majority-voting scheme
REG_TEST_OUT	Output	CMOS (Active HIGH)	Output of the FIFO register with majority-voting scheme
REG_TEST_CLK	Input	CMOS (Active HIGH) (4)	Clock signal for the FIFO register with majority-voting scheme
ERROR	Output	CMOS (Active HIGH)	Flag to indicate an error in the FIFO register with majority-voting scheme
SELECT_bar	Input	CMOS (Active LOW)	Chip selection for pixel disable operations
KILL_PIX_IN	Input	CMOS (Active HIGH)	Input of pixel disable shift register
KILL_PIX_CK	Input	CMOS (Active HIGH)	Clock signal for pixel disable shift register
TEST	Input	CMOS (Active HIGH) (4)	Select test mode for internal threshold and autozero DAC's checks
VDD_Analog	Supply	DC 5.0V	Supply pin for the analog circuitry
REF_Analog	Supply	DC 2.5V	Analog reference-ground
GND_Analog	Supply	DC 0.0V	Ground pin for the analog circuitry
VDD_Digital	Supply	DC 5.0V	Supply pin for the digital circuitry
GND_Digital	Supply	DC 0.0V	Ground pin for the digital circuitry

Notes:

1. The DC operating range of analog inputs is +0.6V to 3.1V with respect to GND.
2. To minimize noise and crosstalk during operation, it is recommended to connect a 10nF ceramic capacitor between pin BIAS_P_S and supply pin VDD_Analog for scintillator channels, and to connect a 10nF ceramic capacitor between pin BIAS_P_X and supply pin VDD_Analog for X-ray channels. If the X-ray channels are not used, shorting pin BIAS_P_X to VDD_Analog will reduce the total supply current. Similarly, when the scintillator channels are not used, shorting pin BIAS_P_S to VDD_Analog can reduce the supply current.
3. To minimize noise and crosstalk during operation, it is recommended to connect a 10nF ceramic capacitor between pin BIAS_N_S and supply pin GND_Analog for scintillator channels, and to connect a 10nF ceramic capacitor between pin BIAS_N_X and supply pin GND_Analog for X-ray channels.
4. On-chip pull-down resistors (≈100kΩ) are implemented on digital inputs POLARITY, SPARSE_SCAN, REG_TEST_IN, REG_TEST_CLK and TEST.

The functional description of the above signals is reported:

AI(0;7): These 8 lines are the inputs of each channel, followed by a semi-gaussian shaping amplifier with 3 μsec shaping time.

AI(8;16): These 8 lines are the inputs of each channel, followed by a semi-gaussian shaping amplifier with 0.5 μsec shaping time.

POLARITY: Select the polarity of the input signal for AI(0,7) channels, (3 μsec shaping time).

SPARSE SCAN: Select the readout mode of the ASIC. In sparse scan selection just the channels triggered within a time window of 2 μsec from the first trigger are readout. In full readout all the channels are readout after a trigger in whatever channel.

GENERAL_RESET: Activating this line lead to the complete reset of the ASIC and Peak and Hold if operating.
The GENERAL RESET application also exclude the CAL function to be active until the first CAL_CLK is emitted.
After GENERAL_RESET all pixels are enabled (kill_pix function reset, see below)

RESET: Activating this line lead to the reset of peak & holds, trigger and related logic.
It is generated by the external circuitry after the processing of data contained into the ASIC. Timing: an ASIC receiving a RESET signal will:
a) If the ASIC has been triggered by one event before receiving this signal then it shall discharge the S&H. Discharge shall be finished within 10 μs from the leading edge of the RESET, then the ASIC shall be ready to receive and detect further events.
b) If the ASIC has NOT been triggered by one event before receiving this signal it shall restore its ability to receive and detect events within 500 ns after the leading edge of RESET.

DISABLE_SH: The DISABLE_SH signal received by the ASIC will:
a) If the ASIC has been triggered by one event before receiving this signal then this function shall disconnect the Peak and Hold stage from the Shaping Amplifier stage and maintain the stored charge in the Hold capacitor.
Further signals at the AI inputs shall have no effect *disconnecting the action of further triggers circuits on S&H.*
The contents of the analogue memories (sample&holds) and of the digital memories (triggered pixel register) are preserved.
b) If the ASIC has NOT been triggered by one event before receiving this signal then this function shall disconnect the Peak and Hold stage and will inhibit any further Sample and Hold operation disconnecting the action of the trigger circuits on the S&H.
The DISABLE_SH line is used just after a valid event (i.e. not veto-ed) in order to allow the extraction of the relevant event data.

PROMPT_TRIGGER: This signal is used to count all detected events, regardless if veto-ed or not (HW rate meter function). This will be used for test and diagnostic purposes both on ground and in flight (background & dead time evaluation).
Timing: the delay from event detection to data_ready activation is composed of two parts:

a) Fixed delay (for Rise Time Protection purposes).
b) Variable delay (due to walk time & jitter in the channel discriminators).

Part b) must is kept below 1 μs (at 3 σ incertitude).

DATA_READY: This line is used to inform the external logic about the presence of data to be read out. The DATA_READY is activated synchronously with the PROMPT_TRIGGER after an event if and only if on the leading edge of the PROMPT_TRIGGER the VETO signal is not activated. The DATA_READY line shall remain active until all active pixels have been readout.
The timing is as precise as discussed for the PROMT_TRIGGER signal from which it is derived.

ENABLE: This line is used to enable the ASIC three-state inputs / outputs one by one during data readout. This feature allows the reduction of connection between AFEE and DFEE through the use of data-busses.
Timing: ENABLE will be received between 1 μsec and 30 μsec from the leading edge of DATA_READY. Data is valid after 200 ns from leading edge of ENABLE.

DATA_ACCEPT: This line is used by the DFEE to prompt a given ASIC to supply the data contents of the "next" active pixel.
The DATA_ACCEPT shall be processed in a given ASIC if, and only if, the ENABLE signal is active on that ASIC (i.e. that ASIC has been selected for readout).
If SPARSE_SCAN is selected, the addressed ASIC works following a "sparse readout" logic, i.e. at the receiving of every DATA_ACCEPT the ASIC shall sequentially put (and latch) at its output the data relating to the active pixel (one or more) only, skipping all the others empty channels in order not to waste readout time.
Timing: Data valid (analogue data settled within 0.5%) at outputs after 500 nsec from DATA_ACCEPT leading edge.

PIXEL_ADDR(0;3): These 4 lines give the address of the current pixel during the readout of the ASIC. They are generated by the ASIC's readout logic.
These are THREE-STATE outputs under ENABLE control.
Timing: Data shall be valid within 500 ns from the leading edge of the DATA_ACCEPT signal.

ANALOGUE OUT: This line is the output of the ASIC's internal analogue MUX.
This signal is a current ranging from 0 to 1 mA proportional to the charge recorded at the input of the current channel on an high impedance (>100Kohm) source.
The current is settled to 0.1 % within 1 μs of the DATA_ACCEPT leading edge.
This line is THREE-STATE output under ENABLE control.

VETO: This input line will be activated typically for times of the order of few μsec when a VETO event is detected in the some external active shield.
It is used as a time-coincidence window: if VETO is active at the leading edge of a PROMPT_TRIGGER then the related DATA_READY is NOT activated, and an ASIC-internal reset routine is performed in order to put the ASIC in its reset status (i.e. waiting for next event). Note that the vetoing of an event does not inhibit the generation of the related PROMPT Trigger.

CAL: This line is used to inject test signals for on-ground calibration purposes. It is assumed that a test capacitor is external connected to the ASIC using this pin.
It shall be held at virtual analog ground when a given chain is selected using the CAL_CK command.
It shall be at GND potential after a GENERAL_RESET (normal operating condition).
This input line shall not be damaged for input voltages within +/- 2.5V from analog ground and injected charge up to 5 pC.

CAL_CK: This line will be used to "clock in" for selection of the test channel.
In normal operation no channel is selected for calibration.
The channel selection shall be performed incrementing the selected channel id# actuating this line with a logic pulse (duration > 1 μs).
The ASIC returns in its normal status (no channel selected for calibration) when it receive a GENERAL_RESET.

THRESH: This line is used to provide each ASIC with a dedicated threshold voltage for its trigger generation stage.
Input impedance > 10 Kohm.

SELECT: This line will be used to select a given ASIC for KILL_PIX operations.

KILL_PIX_IN: This line will be used to load a 16 bit shift register to be used as a command register which states which channels are enabled/disabled.
A "channel enabled" means a channel with enabled triggering function.
This register will be used to "kill" faulty channels (hot spots) that may have their trigger every time active due to some detector malfunction.
It is assumed that the default status at turn-on is that with all channels enabled.
The 16 bit word will be loaded sinchronously with the KILL_PIX_CK
This line shall be operating if and only if the SELECT line is active.

KILL_PIX_CK: This line will be used to "clock in" the data in the above mentioned register.
Clock frequency will be 100 KHz max .
This line shall be active if and only if the SELECT line is active.

SHAPETEST: When active this line exclude the stretcher stage so that at the output of MUX it is possible to observe directly the shaper's output signal.
The Encoder logic commanding the Output Multiplexer shall stay fixed to the last address generated. This feature is used during ground testing. This line is THREE-STATE input under ENABLE control.

OFF_CAL(1,2): *Offset calibration pads.*
INTERNALLY CONNECTED PADS: additional pads for ground supply in order to minimise cross-talk between channels.

5. ICARUS ASIC MODE OF OPERATION

Four main operating modes can be pointed out:

- AUTOCALIBRATION

- ACQUISITION

- READOUT

- SETTINGs

5.1. Autocalibration

This is performed once at ASIC power on. Considering that the minimum signal to be detected is well below the typical offset of CMOS devices, the purpose of an autocalibration is twofold:

1. perform an equalization of the discriminator thresholds over all 16 channels,
2. correct residual channel offsets.

Additionally, the calibration must be performed repeatedly to compensate for offset drifts due to changes in the operating conditions (e.g. temperature) or due to ageing.
During autocalibration, the shaper input is disconnected from the CSA output and connected to the analog ground. Since the shaper exhibits a bandpass characteristic, it is not necessary to include the CSA output offset component into the autocalibration scheme. This prevents signal and noise from affecting the bit decision during the successive approximation algorithm used by the autocalibration procedure.
On each channel, the first correction is made by trimming the shaper output offset so that it comes as close as possible to that of the discriminator. The threshold of the latter is internally set to zero for this purpose and the discriminator itself is used as the decision element in the successive approximation algorithm. To achieve a residual error of less than 0.1% of full-scale, an 8-bit DAC is implemented in each channel. A second correction is necessary to compensate for the offsets of the Peak detector & Hold stage and of the analog output buffer. The op-amp used in the latter operates in open-loop during auto-calibration (i.e. as the comparator in the algorithm). This correction is performed by trimming the offset of the buffer by means of an additional 7-bit DAC (one for all 16 channels).
The first correction is done simultaneously on all 16 channels whereas the second must be realised in sequence (i.e. one channel after the other). The 8+7-bit word auto-calibration information is stored in each channel into data registers specifically designed using triple-latch with majority voting scheme in order to tolerate SEU.

5.2. Acquisition and Readout sequence

After autocalibration, the ASIC works as described in the logic diagram of Fig. 4, where a two-channel event is followed by a single-pulse event which arrives during the readout phase and by a single-pulse veto-coincident event during the following acquisition phase.

For a detected signal the two main operations are ACQUISITION and READOUT

The acquisition mode is related to the ASIC analog signal processing and triggering: it is a mode that is completely under ASIC control, apart from the RESET pulse which is externally supplied to start the process.

The readout mode is related to the data collection: this mode is under the control of the external electronics, the ASIC shall actuate commands and shall use its sparse readout logic to provide the data when asked for.

NOTE: in Fig. 4 and in the following the ASIC I/O signals are represented by their name in capital characters while some ASIC internal signals are represented in lowercase letters.

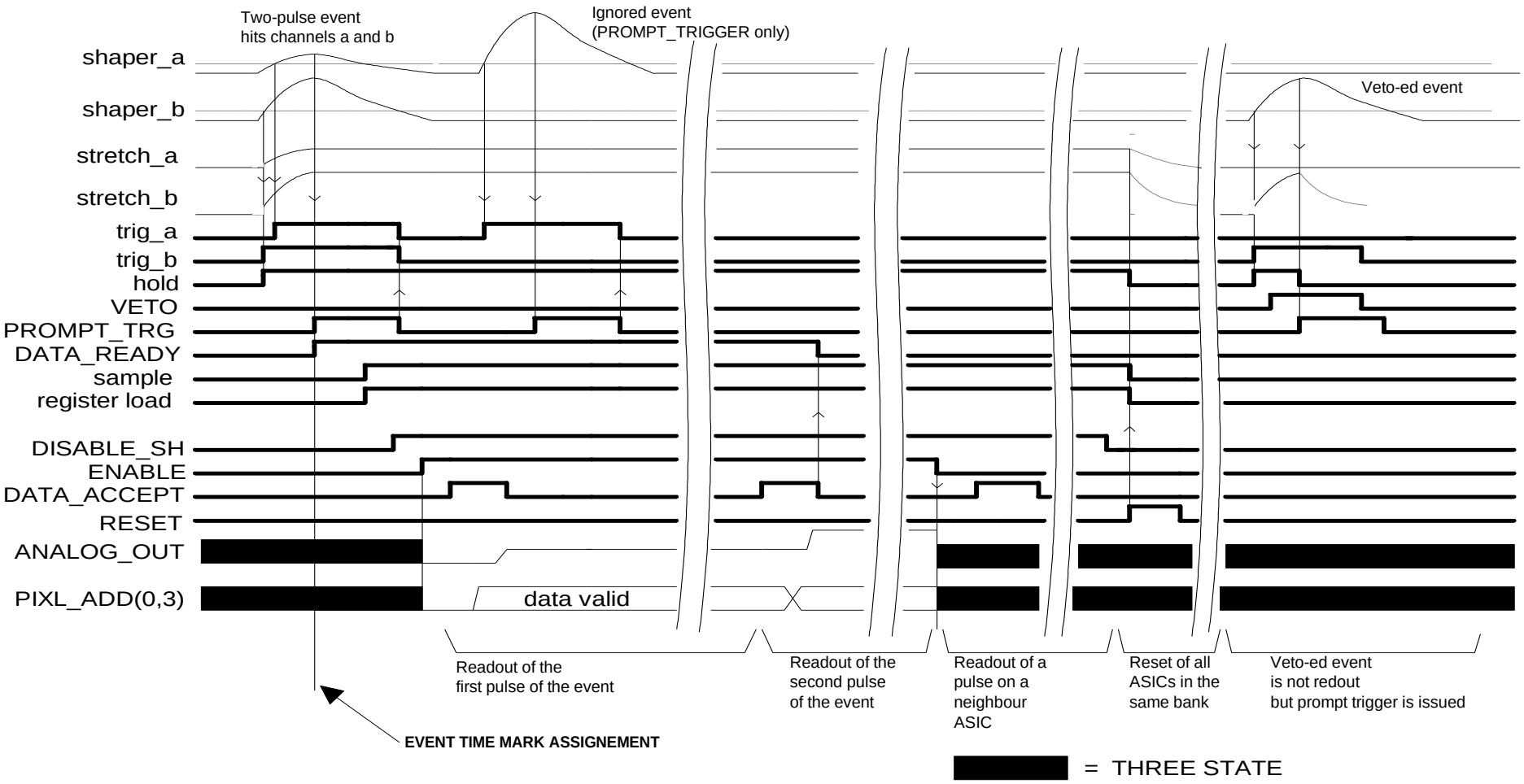

Fig. 4 ASIC Logic state diagram

5.2.1. Acquisition

In operating condition the 16 ANALOG_INPUT of the ASIC will be subjected to a random sequence of charge pulses with a TBD average rate (Poisson distribution).
Most of these pulses will arrive as a single-channel pulse, but double or higher multiplicity pulses will also be present in a low percentage, the ASIC is anyway designed in order to process up to 16 channel pulses at the same time (one pulse per channel).
At the same time the VETO digital input is subjected to a random sequence of pulses with duration TBD μsec and TBD KHz average rate (Poisson distribution).
The general behaviour of the ASIC in the acquisition mode is follows:

1) The pulses above the THRESHOLD value activates the PROMPT_TRIGGER pulse.

2) If at the activation of the PROMPT_TRIGGER the VETO signal is active then nothing else happens and the ASIC reset itself and return in the acquisition mode.

3) If at the activation of the PROMPT_TRIGGER the VETO signal is not active then:
IF and only IF the ASIC is not already loaded with previous data, the ASIC activates the DATA_READY and subsequently stores the pulses data (address and amplitude).
The raising of the DATA_READY mark the passage from the acquisition mode to the readout mode.

4) If a pulse arrive while the ASIC is already in readout mode (i.e. is undergoing readout sequence of previous pulses) then it activates the PROMT_TRIGGER pulse only.

5) if a VETO arrive while the ASIC is in readout mode (DATA_READY is active) then it has no effect.

With reference to Fig. 4:
starting with the two-pulse event (note that the discriminator signals trig_a and trig_b fire at different times) the first of them starts the internal "hold" signal so that the Peak& Hold outputs stretch_a and stretch_b begin to follow the leading front of the shaper-output signals.

A sketch for the Peak & Hold logic is represented in the overall ASIC schematics of Fig. 1: it includes a two switches commanded by the Sample and Hold logic inside the ASIC. In normal operations the two switches are closed and the hold function is inhibited. The Hold switches of all the ASIC's channels are commanded by the OR of all the Triggers and are opened at the firing of the first triggered channel.

The Sample switches are commanded by the ASIC after a fixed delay from the leading edge of the DATA_READY: the delay between this edge and the Sample is long enough to act as Rise Time Protection for the channels. Hold and Sample are released at the end of the processing operations. The PROMPT_TRIGGER is activated at a time not dependent from pulse amplitude corresponding to the peak of the shaped pulse.

The trailing edge of the PROMPT_TRIGGER pulse de-activate all the trig_# lines.

The DATA_READY shall be activated synchronous to the PROMPT_TRIGGER.

Following the DATA_READY activation the ASIC, after 5 μs time for rise-time protection, stores the following data:

1) analog data inside the Peak&Hold

2) digital data inside a 16 bit register to take a record of which channel has been activated.

5.2.2. Readout mode

The readout sequence is driven by the external circuitry following the detection of the active DATA_READY.
NOTE: DATA_READY is the only signal that prompt the external circuitry about the presence of data inside the ASIC, it includes a very time-precise leading edge as it is that edge which will be used for the event time-marking.

After the receiving of the DATA_READY the external circuitry will start the following sequence:

1) after 1 μs waiting the external circuitry will activate the DISABLE_SH line. Basically, at this time, all data are frozen inside the ASIC.

2) in a time from 0 to 30 μs from point 1) the external circuitry will activate the ENABLE line: the ASIC connects all its THREE STATE I/O as driver or receiver on the related lines.

3) After 250 ns the external circuitry will then activate the DATA_ACCEPT line for 500 ns:
The ASIC puts at its output the data relating to the first channel to be readout.
The data are valid within 500 ns from the DATA_ACCEPT leading edge.
The ASIC shall select the channel to be readout depending from the readout schema.

4) The data at ASIC output shall remain valid until a new DATA_ACCEPT is issued.

5) At the receiving of a new DATA_ACCEPT the ASIC puts at its output the data relating to the next channel to be readout.

6) The sequence go on until all "active" channel have been readout.
When asked for its last "active" channel the ASIC shall de-activate its DATA_READY line on the trailing edge of the DATA_ACCEPT.

7) After last active channel readout the external logic will de-activate the ENABLE:
The ASIC THREE-STATE I/O goes in high impedance outputs and not-active inputs.
DATA_ACCEPT pulses will continue to arrive but has no effect.

8) The ASIC shall stay in the present situation until the DISABLE_SH is active.

9) After completing the ASIC bank readout the external circuitry will send a RESET pulse.

10) The ASIC shall be ready for a new acquisition sequence.

5.3. SETTINGs

5.3.1. Channel (or pixel) exclusion sequence

The pixel exclusion sequence will be run in order to inhibit the triggering action of some channel of the ASIC.
The sequence would be as follows:

a) The ASIC kill_pix function is enabled activating the SELECT line

b) a 16 bit "kill" word is clocked in the ASIC using the KILL_PIX_IN serial input and KILL_PIX_CK: the data will be put at the KILL_PIX_IN at the leading edge of the KILL_PIX_CK, it shall be transferred into the first stage of the ASIC shift register at the trailing edge of the KILL_PIX_CK.
After 16 of above cycles the 16 bit "kill" word is inside the ASIC.

c) on the trailing edge of the SELECT the loaded word is latched and from now on the trigger function shall be inhibited for those channels related to a "1" (TBC) state-bit of the "kill" word.

d) the above status is maintained until a GENERAL_RESET is given.

5.3.2. Internal threshold check

Internal Threshold Check which is intended to measure the actual internal threshold of a selected channel.

5.3.3. Internal register test

Internal Register Test which gives an insight into the contents of the ASIC registers.

5.3.4. Test shape

For testing purposes the output signal from the sh-amp of a selectable channel can be directly observed at the ANALOG_OUT pin with a proper setting of commands.

6. ICARUS-SDC operation test and performances

The basic ASIC behaviour have been evaluated using the test set-up depicted in Fig. 5.

The ASIC was placed on an evaluation board which includes the power filtering, the threshold generation and the REF (+2.5V) generation and filtering. The evaluation board carries also all the circuits which are in charge of the CMDO to CMOS and CMOS to RVS conversion for easier connection to the external equipment.

In alternative to the SDC a Pulse Generator can delivered a signal to the ASIC input.

The ASIC was commanded with a Pattern Generator and the output was send either to a Multi Channel Analyzer (MCA) or a mixed Analog and Digital oscilloscope.

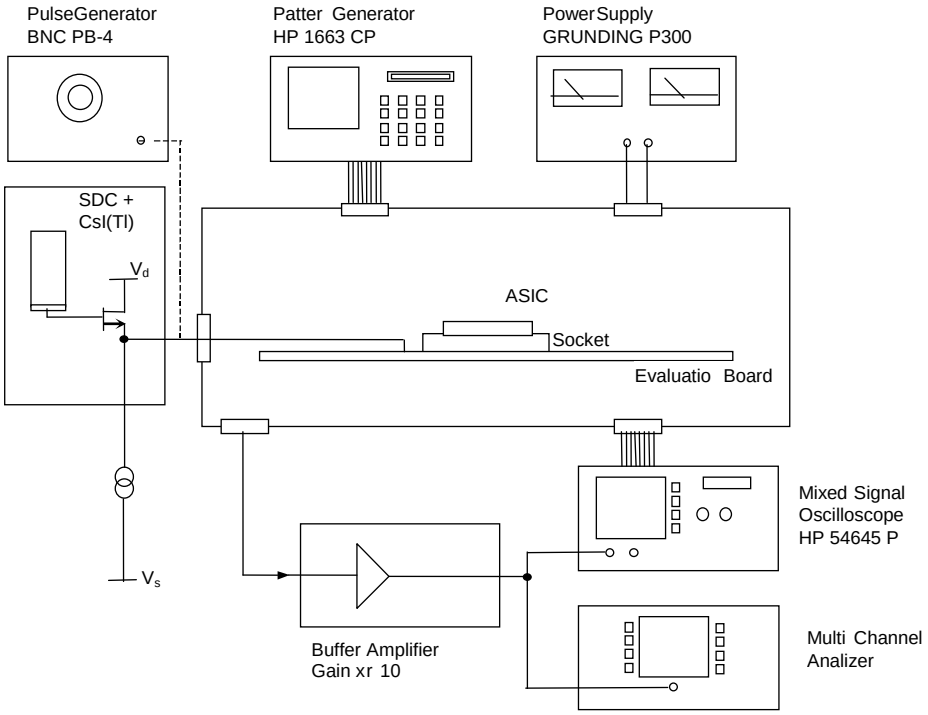

Fig. 5 ICARUS-SDC ASIC test set-up

6.1. Operations

In Fig. 6 the main signals of a typical self-triggering and read_out sequence has been registered on the oscilloscope.

In Fig. 7 the output signals from the two chains with different shaping time are shown; in this case the input signal was delivered by the pulser.

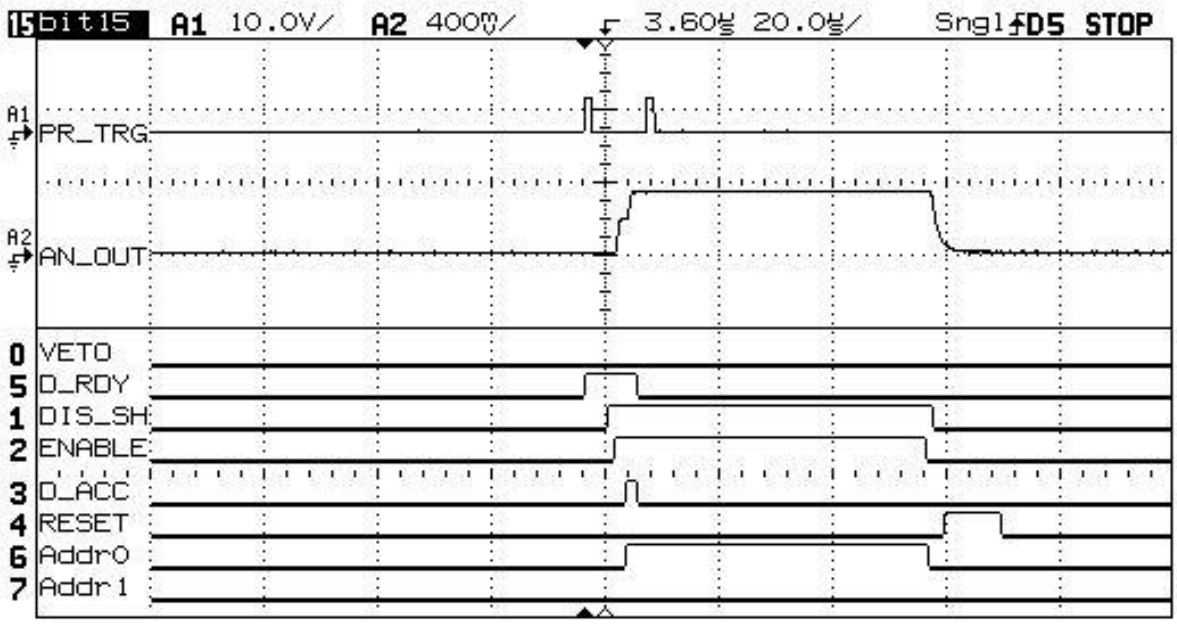

Fig. 6 Read Out sequence for a detected event on one channel (Channel 1 , just 2 of the 4 address bit are shown)

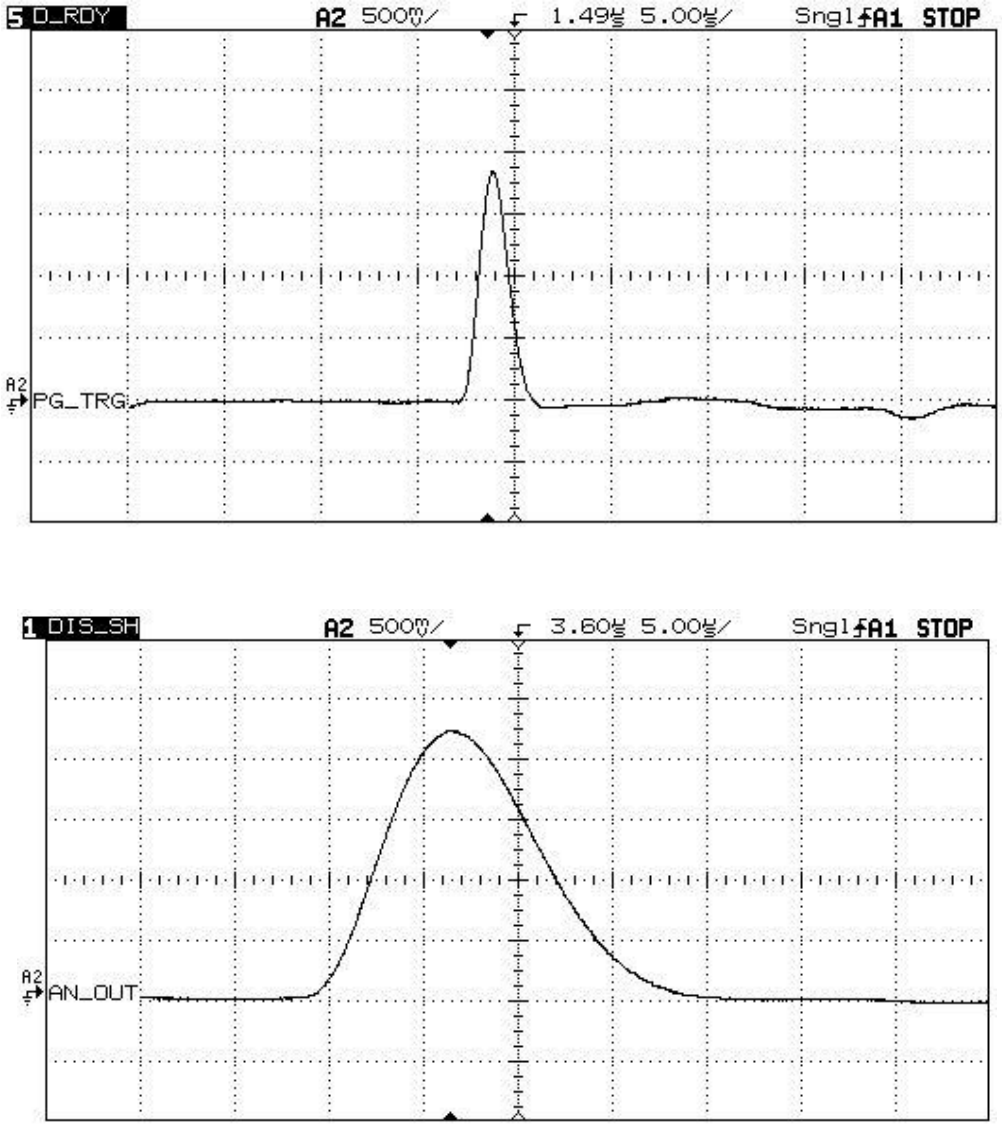

Fig. 7 Top: shape of the output pulse for the direct detection branch of the ASIC (peaking time ~ 1.5 μs) with the ASIC was configurated in its shapetest function.

Bottom: Shape of the output pulse for the scintillator branch of the ASIC (peaking time ~ 7μs) with the ASIC configurated in its shapetest function.

6.2. ASIC Analog chain main characteristics

The main characteristics measured for a typical ASIC chain (slow channel) are reported on the following.
The characteristic of the PD detector used are: active area 10 mm2, thickness 300 μm, leakage current @ 20 °C 1 nA.

Gain	42
Noise	14 μV rms
Linearity	± 1 %
Dynamic range	~ 1000
Power / channel	6.25 mW
Jitter and walking time on D_RDY	1 μs

7. EXAMPLE OF ICARUS_SDC USE

As an example of ICARUS_SDC use a system made up with two ASIC and 8 SDCs has been tested, the SDC were intended for a later use with a scintillating crystal, so the slow channels of the ASIC were used.

For noise evaluation purposes, the SDC without crystal were mounted on an AFEE board and illuminated with a non-collimated ^{241}Am source.

The eight spectra obtained analysing the files are shown in Fig. 8 .

Seven 300 μm thick SDCs and a 450 μm thick SDC have been used. The 450 μm thick device was connected to channel 5 of ASIC 5, and exhibits poorer spectroscopic performance than the other devices.

An average 2.2 % energy resolution FWHM at 59.54~keV has been obtained for 300 μm thick devices, while it is 4.2 % for the 450 μm thick one. These worse performance is expected to be due to the larger thickness that enhances the parallel noise contribution especially at shaping times higher than the optimum. In fact, it must be noted that the shaping time used in this application is ~ 3 μs. Such a shaping time is needed for scintillation detectors to account for the few μ s CsI(Tl) scintillation light decay time and avoid ballistic deficit, but is higher than the optimum shaping time required for SDD operation as a direct X-ray detector (about ~ 0.5 μs) that allows better noise performance.

An average equivalent noise charge) of about 120 e^- rms has been obtained for the 300 μm thick devices; the detector connected to channel 6 of ASIC 6 exhibits an ENC of 108 e^- rms while, with standard laboratory electronics and the same shaping time, an ENC equal to 80 e^- was obtained. This means that front-end electronics was not completely optimised.

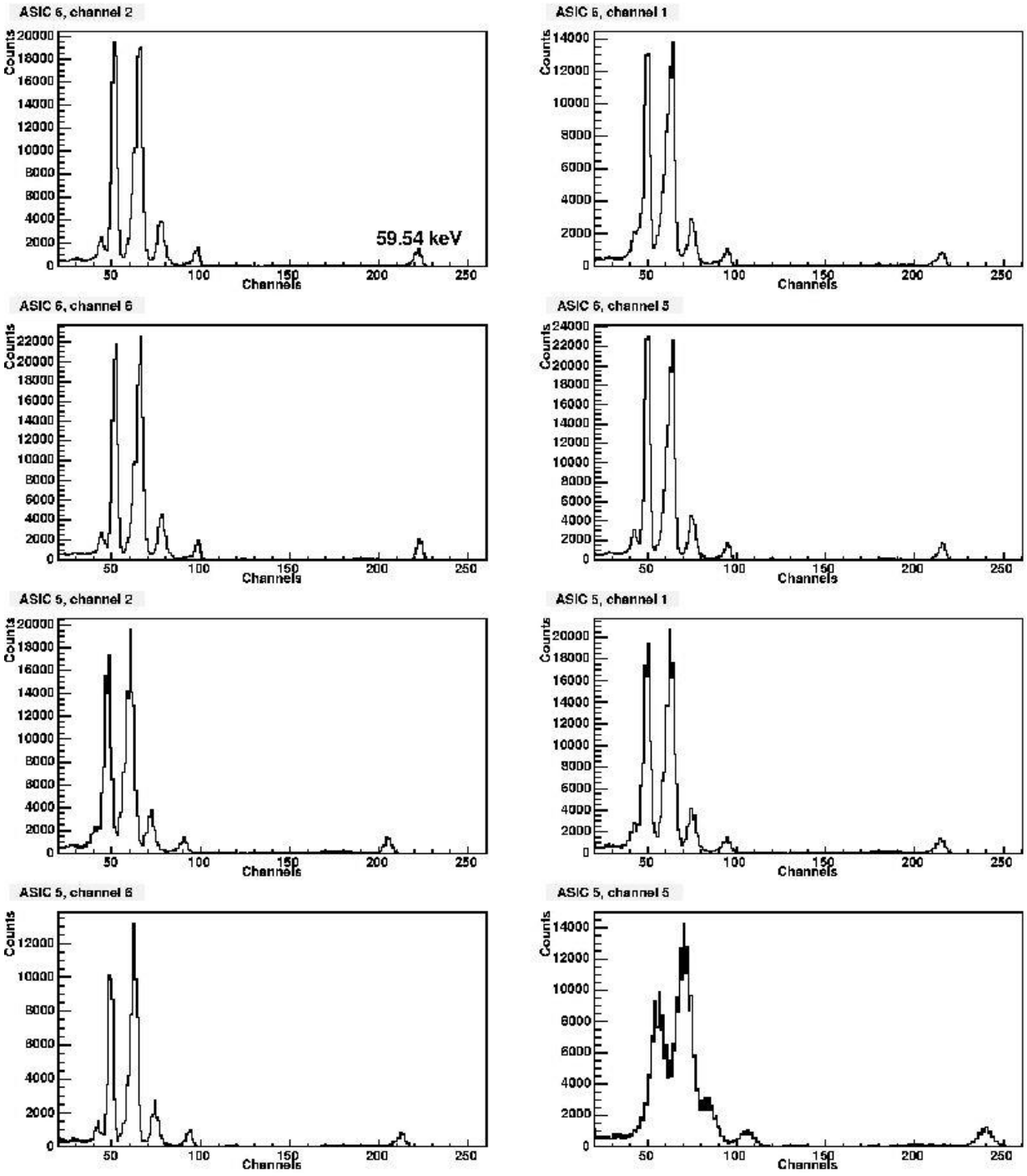

Fig. 8 ^{241}Am spectra of the detectors coupled to 8 channels of the instrument. For each detector, the corresponding channel (from 0 to 7) and ASIC number (either 5 or 6) used is indicated.

8. ICARUS_SDC AND SPACE QUALIFICATION REQUIREMENTS

The ICARUS_SDC ASIC has been realised in accordance to ESA/SCC 9000 Generic Specification.

To increase the resistance to SEU all the ASIC's digital register are redundant and operate on a majority vote scheme.

The ICARUS_SDC ASIC is derived by the ICARUS chip that is actually in operation on the INTEGRAL satellite.

ICARUS is able to withstand the following physical environment

- Operating temperature range with maintaining of characteristics -10 to 50 °C

The dynamic parameters have been verified against operating temperature range whilst static parameters have been verified against military temperature range (i.e. -55 °C + 125 °C).

Radiation hardness total dose: 5 KRad

SEL (Single Event Latch-up) sens. > *70 MeV/mg/cm^2*

SEU (Single Event Upset) sens. > *30 MeV/mg/ cm^2*

9. FURTHER DEVELOPMENTS

Starting from ICARUS_SDC ASIC, a further development will be achieved with the RUA ASIC that has been conceived so that it will include a number of electronic chains for gamma ray spectroscopy.
The first active component of each chain is not included in RUA but it has to be mounted on the detector itself.
All the digital functions as ADC, time marking etc are realised inside the chip.
Finally the setting of the main parameters of each chain is extremely flexible.

9.1. THE RUA ASIC

A RUA channel, Fig. 9, includes five main blocks: an input amplifier, a shaping amplifier, a programmable gain amplifier (PGA) with polarity selection and a fine selectable gain, the peak and hold with the threshold discriminator and finally the ADC.
The Input Amplifier has a two blocks structure with an overall selectable gain of 1, 2, 5 or 10.
The Shaper Amplifier is designed to optimize the signal to noise ratio for different kind of detectors allowing the selection of the peaking time between 0.5, 1, 3 and 6 μs. Fine tuning of the time constant can be done, for a selected peaking time, with an 8 bit command register, that changes the value of capacitors in the $CR(RC)^2$ filtering function. Moreover the pole zero compensation of the circuit is also selectable to compensate decay time constant of 0.1, 0.2, 0.5, 1 and 2 ms via another 8 bit command register. The Programmable Gain Amplifier can range from 1 to 2 with a 10 bit resolution; this circuit is based on an amplifier to which the signal is connected via a resistive DAC. This stage has been included to allow the equalization of detectors with different response. The peak and hold is enabled by the discriminator whose threshold level is selectable with an 8 bit precision DAC. Finally the ADC has a 10 bit successive approximation architecture and operates with 1 MHz clock. In order to minimize digital noise on the chip, the ADC and its clock start to work just if an event has been detected

RUA has three operative modes: Setting - Acquisition - Readout
In setting mode the internal registers for setting all the parameters will be filled. This mode will be operated at RUA switch on.
In acquisition mode RUA will operate collecting signal delivered by the detector. The input signal will be elaborated, converted in digital form and stored for readout.
In readout mode the datum will be transferred to the external.

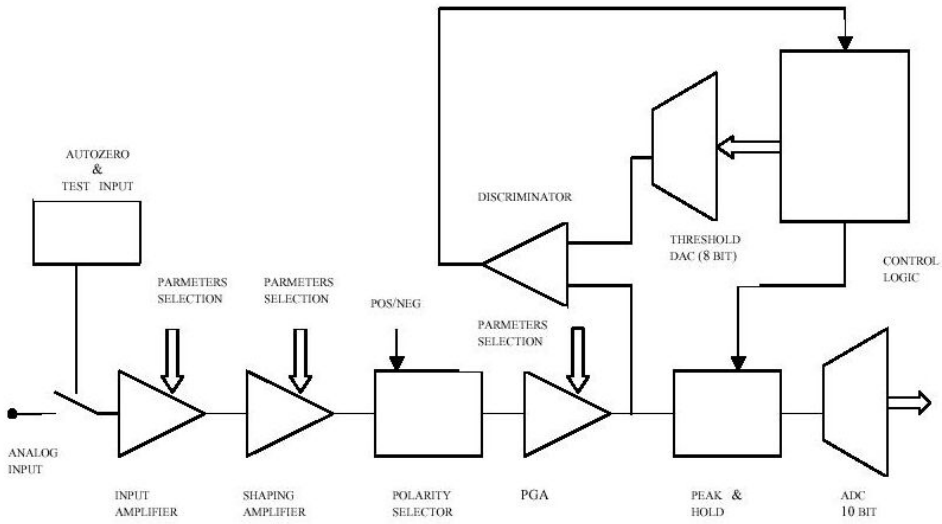

Fig. 9 Functions realized on a RUA one channel.

RUA ASIC test

RUA prototype was realized using Multi Project Wafer (MPW) opportunities at AMS foundry with CMOS 0.8 μm technology; the channel area is 3.3 mm^2.
The ASIC has been mounted on a test board and connected to laboratory equipments as power supply, pulse generator, memory oscilloscope and Multi Channel Analyzer (MCA). The registers for programming the operation of the main blocks are 45 as described in Table 1.

Parameter	Value	
Signal polarity input	negative or positive	
Input Amplifier gain	1 - 2 - 5 - 10	v/v
Shaper peaking time	0.5 - 1 - 3 - 6	μs
Fine peaking time adj.	15 ÷ 25 (2^8 step)	pF
Pole-zero cancellation	0.1 - 0.2 - 0.5 - 1 - 2	ms
Fine gain stage	1 ÷ 2 (2^{10} step)	v/v
Discriminator range	0.1 ÷ 0.3 (2^8 step)	V
Rise time protection	2 - 3 - 6 – 10 - 12	μs

Table 1 RUA main parameter selection

A short description of the behavior of each RUA block is reported in the following.

Input amplifier: It has been built with four (1-2-5-10 V/V) coarse gain selection. The operation of this stage exhibits correct results for all the gain setting with positive and negative polarity input.

Shaping Amplifier: The functionality of this stage is shown in Fig. 10; the same input signal has been shaped with the four allowed different rising times; in each case the pole zero cancellation was optimised. The four shapes have been stored on the digital scope at different times, and displayed all together for comparison. For each of the selectable peaking times, acting on the fine tuning of the shaping amplifier, the peaking time ranges have been measured to cover with continuity all the values.

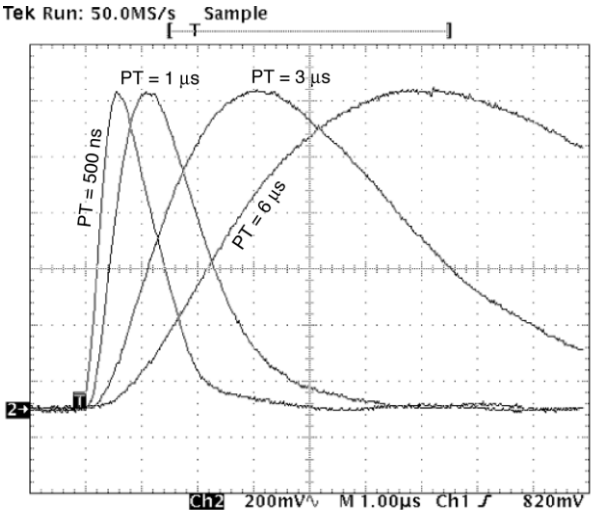

Fig. 10 Output of the Shaping amp for different settings

Programmable Gain Amplifier (PGA): A selected number, one for each bit of the DAC register, of the 2^{10} steps of selectable gain of this stage that operate in the range between 1 and 2, has been tested and proved to be correct. The same is for the functionality of the signal polarity selection. The overall chain was also tested for big saturated signals and in this case no bad behaviour or oscillation were noticed.

Amplitude Discriminator: The discriminator compares the shaped signal with a voltage level threshold that spans from 100 to 300 mV selectable with an 8 bit DAC threshold adjustment. The logical signal from the discriminator is used to enable the peak and hold for the acquisition phase.

Peak detector and Hold and ADC: The Peak and Hold circuit automatically detects the maximum of the shaped signal. To avoid pulse pile up this stage is disconnected from the shaper after a selectable Rise Time Protection (RTP) interval. After the RTP the ADC is enabled to convert.

The circuits of the RUA prototype satisfy the design goals in terms of functionality and flexibility. The noise performances and the linearity are as expected for all the peaking times but the 6 μs one; this feature will be further investigated.

An improvement in the RUA design could be made reducing the time jitter of the discriminator operating a change on this block.