

# POLCA2 (POLarimetry with CZT Arrays): experimental set-up, calibration procedures and results.

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## 1. Aims and summary

This document describes the experimental set-up and the preliminary results of the measurements performed with an X-Ray detection system based on a 16x16 pixel CdZnTe detector from Imarad coupled to a Front-End readout based on ASICs from eV products. The experimental activity main goal is to extract evaluations of the polarization detection capability of the CZT detector induced in the crystal by primary polarized 100 keV÷1MeV photons at the European Synchrotron Radiation Facility (ERSF) in Grenoble, France. Preliminary tests shall also be performed at Ferrara University with the 10÷100 keV polarized beam able to qualify a Laue X-Ray focalizing lens prototype.

There have been very few developments in the field of polarimetry in hard X- and soft  $\gamma$ -ray astronomy, indeed not one dedicate polarimeter has ever been launched either as a satellite or balloon borne experiment.

The collaboration developed between the Physics Department of the University of Coimbra, Portugal and the IASF/INAF–Dept. of Bologna (*Istituto di Astrofisica Spaziale e Fisica Cosmica*), Italy, have recently proposed an instrument devoted to polarimetric measurements for hard X-ray and soft gamma ray (100 keV – 10 MeV) astrophysical measurements. The proposed telescope, using four  $32 \times 32$  matrices of thick CdTe micro-spectrometers (2 mm × 2 mm × 10 mm) as the detection plane will allow this type of measurement to be performed for the first time by a dedicated instrument whose detection plane is optimised for the detection of Compton scattered events.

As part of the design process, a sophisticated Monte Carlo simulation code based on the GEANT4 program was developed, and an extensive polarimetric study was performed in order to evaluate the response and performance of the detection plane to the type of linearly polarised radiation expected to be produced by physical processes inherent to celestial sources.

In order to compare the results already obtained from detection plane Monte Carlo simulations with experimental data, a first experimental run (POLCA1) has been performed by using a CdTe prototype matrix ( $4 \times 4$  pixels) detector. The data extracted in the first run (POLCA1) encouraged to develop a second experimental set-up (POLCA2) based on a CZT 16x16 pixel detector.

The system should provide coded data able to perform spectroscopic analysis on one or two CZT pixels coincident within a selectable acceptance time (about 1 µsec).

The detection system is implemented with:

- a front-end (FE) electronics able to analogically process up to 122 channels;
- a conventional wired red out electronics (Takes) with 128 channel capability, coincidence circuitry and digital-to-analog converter (10-bit ADC);
- a data collecting system (PC) operating under user written SW in LabView environment.

The report should provide a technical tool both to arrange the experiment preparation and provide the user with the documentation useful to inspect for fault search or to modify the existing set-up.



# 2. The CZT detector

The Imarad CZT detector is organized in 16x16 pixel array; each square pixel having dimensions of 2mmx2mm with an interpixel gap of 0.5 mm. The pixel (anods) CZT are presented at the output user through the connectors J1, J2, J3 (0.5 mm interpin gap, Matsushita/Panasonic) wired on the anode side. J1 and J2 are 50+50 pin, J3 is 70 pin. Since 128 pixels as a maximum can be read out, the connector J3 is not used.

A schematic view of CZT detector and the I/O harness is shown in Fig. 1.



Fig.1. Organization of the 16x16 Imarad CZT detector and I/O connectors.

The following three lists give the pin function of the output connectors J1, J2, J3 both in the Imarad coding (alphanumeric) and in the pixel numbering (purely numeric ranging from 1 to 128).



Connector J1-100 pin											
Pin #		Pixel #	Pin #		Pixel #						
1	P16	224	2	K15	159						
3	P15	223	4	K16	160						
5	<b>T16</b>	256	6	K14	158						
7	T15	255	8	K13	157						
9	<b>R16</b>	240	10	L16	176						
11	R15	239	12	M16	192						
13	R14	238	14	L15	175						
15	R13	237	16	N16	208						
17	P14	222	18	M15	191						
19	P13	221	20	N15	207						
21	T14	254	22	L14 (?)	174						
23	T13	253	24	M14	190						
25	P12	220	26	L13	173						
27	R12	236	28	N14	206						
29	T12	252	30	M13	189						
31	P11	219	32	N13	205						
33	R11	235	34	M11	187						
35	T11	251	36	M12	188						
37	P10	218	38	N12	204						
39	R10	234	40	M10	186						
41	T10	250	40	MQ	185						
43	TQ	230		N11	203						
45	R0	233	46	N10	203						
43	PQ	233	48	NO	202						
47	T8	217	50	N8	201						
51	<b>R</b> 8	232	52	M	184						
53	<b>P</b> 8	232	54	N7	104						
55	T7	210	56	N6	108						
57	R7	231	58	M7	183						
59	P7	215	60	M6	182						
61	T6	246	62	K5	1/10/2						
63	R6	230	64	M5	181						
65	D6	230	66	KA	1/18						
67	T5	217	68	N5	107						
60	15 P5	243	70	16	166						
71	D5	213	70	N/	100						
73	T 4	213	74	114	165						
75	14 D4	244	74		105						
73	R4 D4	210	70	T A	164						
70	Г4 Т2	212	70		104 Not wood						
/9 01	15 D2	245	82		Not used						
81 82	KJ D2	227	84		Not used						
03 05	r5 T2	211	04 96	1D2 1D2	Not used						
00	14 D2	242	00	ID5	TNOT USED						
0/	K2 D2	210	00		195						
89 01	<u>r</u> 2	210	90	LJ	103						
91	11 D1	241	92	IVI J NO	1/9						
93	KI D1	225	94	INZ MO	179						
95	PI N1	209	90		178						
9/		195	98		102						
99	Ml	177	100	LI	161						



Connector J2-100 pin											
Pin #		Pixel #	Pin #		Pixel #						
1	J15	143	2	G16	112						
3	H15	127	4	F16	96						
5	J14	142	6	E16	80						
7	H16	128	8	G14	110						
9	H14	126	10	F14	94						
11	J16	144	12	J13	141						
13	K12	156	14	J12	140						
15	K11	155	16	F15	<b>95</b>						
17	K10	154	18	G15	111						
19	L12	172	20	J11	139						
21			22	H11	123						
23	L11	171	24	H13	125						
25	F10	90	26	G13	109						
27	H7	119	28	J10	138						
29	K8	152	30	H10	122						
31	L10	170	32	H9	121						
33	<b>G8</b>	104	34	<b>J9</b>	137						
35	K9	153	36	H12	124						
37	H8	120	38	<b>J8</b>	136						
39	F7	<b>87</b>	40	G12	108						
41	L9	169	42	F13	93						
43			44	<b>F12</b>	92						
45	L8	168	46	<b>G9</b>	105						
47	K7	151	48	G11	107						
49	H5	117	50	F11	91						
51	<b>G7</b>	103	52	G10	106						
53	K6	150	54	<b>E</b> 11	75						
55	L7	167	56	<b>F8</b>	88						
57	J5	133	58	E10	74						
59	J4	132	60	G5	101						
61	<b>J7</b>	135	62	<b>F9</b>	<b>89</b>						
63	H6	118	64	<b>E9</b>	73						
65	CGND	Shield	66	<b>G4</b>	100						
67	CGND	Shield	68	<b>J6</b>	134						
69	CGND	Shield	70	F2	82						
71	CGND	Shield	72	H4	116						
73	CGND	Shield	74	<b>G6</b>	102						
75	CGND	Shield	76	<b>G3</b>	99						
77	ID4	Not used	78	<b>F6</b>	86						
<b>79</b>	H3	115	80	<b>E2</b>	66						
81	<b>J</b> 3	131	82	<b>E6</b>	70						
83	AGND	Not used	84	J2	130						
85	K3	147	86	F5	85						
87	H2	114	88	<b>E5</b>	<b>69</b>						
89	H1	113	90	<b>E4</b>	68						
91	<b>K1</b>	145	92	F4	<b>84</b>						
93	<b>J1</b>	129	94	<b>G2</b>	<b>98</b>						
95	K2	146	96	<b>E3</b>	67						
97	<b>F1</b>	81	<b>98</b>	<b>F3</b>	83						
99	<b>G1</b>	<b>97</b>	100	<b>E1</b>	65						

#### $\mathbf{a}$ TO 100



		Connect	or J3-7(	Connector J3-70 pin											
Pin #		Pixel #	Pin #		Pixel #										
1	C16	<b>48</b>	2	A16	16										
3	B15	31	4	A15	15										
5	C15	47	6	A14	14										
7	C14	46	8	B16	32										
9	D16	64	10	C13	45										
11	D15	63	12	B13	29										
13	D14	62	14	<b>B14</b>	30										
15	E14	<b>78</b>	16	A12	12										
17	E15	<b>79</b>	18	B12	28										
19	D13	61	20	A11	11										
21	C12	44	22	A13	13										
23	E13	77	24	<b>C9</b>	41										
25	E12	<b>76</b>	26	D9	57										
27	D12	60	28	A10	10										
29	<b>C11</b>	43	30	A9	9										
31	<b>B11</b>	27	32	<b>C8</b>	<b>40</b>										
33	D11	<b>59</b>	34	<b>B9</b>	25										
35	<b>D10</b>	<b>58</b>	36	<b>B8</b>	24										
37	<b>C10</b>	42	38	A8	8										
39	<b>B10</b>	26	40	<b>C7</b>	39										
41	<b>D8</b>	56	42	A7	7										
43	<b>D7</b>	55	44	A6	6										
45	<b>B6</b>	22	46	<b>B5</b>	21										
47	<b>C3</b>	35	<b>48</b>	A5	5										
49	<b>C6</b>	38	50	A4	4										
51	<b>B7</b>	23	52	<b>B3</b>	19										
53	<b>D6</b>	54	54	A3	3										
55	<b>C5</b>	37	56	<b>B2</b>	18										
57	D5	53	58	A2	2										
59	<b>E8</b>	72	60	<b>C4</b>	36										
61	<b>E7</b>	71	62	<b>C2</b>	34										
63	<b>B4</b>	20	64	A1	1										
65	D3	51	66	<b>B1</b>	17										
67	<b>D4</b>	52	68	<b>C1</b>	33										
69	D2	50	70	D1	49										

The distribution of the CZT pixels in the I/O connectors is shown in Fig 2. The connector J1 outputs 96 pixels, J2 90, J3 70. The combination of J1 and J2 permits to read up to 186 pixels. As already told, the Takes processing electronics permits to read out up to 128 pixel; since the main constraint dictates a square (11x11) CZT pixel subset is considered, it is required that:

- it is mandatory to connected J2 because it permits to wire the internal CZT detector shieldings to the analog GND of the front-end electronics;
- ▶ the couple J2-J3 does not permits to read a 11x11 adjacent pixel subset:
- the couple J1-J2 is chosen for the read out of the detector; ►
- the connector J3 is left unused. ►

The election of the couple of connectors J1-J2 permits to read out a square CZT subset of 11x11 pixels arranged as depicted in Fig. 3.



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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
13	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
03	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
odd	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80
i i	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96
12	97	98	99	100	101	102	103	104	105	1 <b>0</b> 6	107	108	109	110	111	112
J <i>2</i>	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128
	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144
odd	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160
	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176
	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192
j	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208
11	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224
01	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240
odd	241	242	243	244	245	246	247	248	249	250	<b>2</b> 51	252	253	254	255	256

Fig. 2. CZT pixel distribution in the output connectors J1, J2, J3.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	A
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	в
48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	Ċ
64	63	62	61	6 <b>0</b>	59	58	57	56	55	54	53	52	51	50	49	D
80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	Ê
96 J2/4	95 J2/16	94 .12/10	93 J2/42	92 .12/44	91 J2/50	90 J2/25	89 J2/62	88 J2/56	87 .12/39	86 J2/78	85 J2/86	84	83	82	81	F
112 12/2	111 112/18	110	109 .12/26	108 .12/40	107	106 J2/52	105 J2/46	104 .12/33	103 .12/51	102 12/74	101 J2/60	100	99	98	97	G
128 J2/7	127 .12/3	126 .12/9	125 J2/24	124 J2/36	123 .12/22	122 .12/30	121 J2/32	120 J2/37	119 .12/27	118 J2/63	117 .12/49	116	115	114	113	ĺн
144 12/11	143 12/1	142	141	140	139	138	137	136	135	134	133	132	131	130	129	J
160 .11/4	159 .11/2	158	157 .11/8	156	155	154	153	152	151	150	149 .11/62	148	147	146	145	ĸ
176 .11/10	175 .11/14	174	173 .11/26	172	171	170	169	168	167	166	165 .11/74	164	163	162	161	L
192 1/10	191 1/14	190 11/24	189 11/20	188 11/26	187 1/24	186 11/40	185	184 11/52	183 11/59	182	181 1/64	180	179	178	177	<b>ј</b> м
208 11/12	207 11/20	206	205 11/32	204	203 11/44	202 11/46	201 11/48	200	199 1/54	198 1/56	197 1/68	196	195	194	193	N
224	223	222	221 .11/19	220	219 .11/31	218 .11/37	217 .11/47	216 .11/52	215 .11/59	214 .11/65	213	212	211	210	209	P
240	239 11/11	238	237	236 11/27	235 11/22	234	233 11/45	232	231 11/57	230 11/62	229	228	227	226	225	R
256 JI/5	255 JV7	254 J1/21	253 JI/23	252 .II/29	251 JI/35	250 J1/41	249 J1/43	248 JI/49	247 JI/55	246 JI/61	245 J1/67	244	243	242	241	Т

Fig.3. CZT Pixel subset (low left hand corner) selected for the experiment. Pixels are also related to the J1-J2 output pin number.



Fig. 4 shows the details of the J1-J2 output pin connection assembled at the factory, the association with the pixel numbering (Fig. 2&3) and the grouping of the pixel signals relative to the destination FE ASICs (8, 16 channel eV ASICs are used).



Fig. 4. CZT subset chosen for the read out and pixel association with the 8 eV ASICs.

The use of the eV ASICs, each of which analogically processes 16 CZT channels, permits-in combination with the associated Takes electronics and the acquisition system-to accumulate two



coded events coincident within the acceptance time. So, even if somewhat pletoric and expensive, the experimental set-up permits both photon-by-photon spectroscopy and polarimetric studies.

# **3.** The Front-End electronics

A dedicated PCB has been designed and developed for the FE electronics (8, 16 channel ASICs from eV products) by simply reproducing a PCB design constructed for another application requiring the use of a single eV ASIC (16 analog channels). The implementation (Fig. 5) was been found reliable and has been also adopted as basic active component for the present application.



Fig. 5. Basic electric configuration for an eV, 16-chs ASIC. A LT1763 LDO regulator is used to bias two ASICs, which means that in the final PCB there are 4 regulators.

In Appendix I are reported the electrical schemes of the 4 couples of ASICs, each couple being powered by an LT-1763 regulator.

Fig. 6 shows the component side view of the 8-ASICs PCB. By acting on couples of on-board jumpers (JPi, JPi+1), any ASIC's gain and peaking time can be independently regulated: possible values are listed in Table I.



1 401		s gain and	peaking time values for	setting	
Gain (mV/fC)	JPi		Peaking Time (µsec)	JP	i+1
	LSB	MSB		LSB	MSB
200	0	0	0.6	0	0
100	1	0	1.2	1	0
50	0	1	2.4	0	1
33	1	1	4	1	1

Table I: ASIC's gain and peaking time values for setting

Jumpers JPi and JPi+1 open select Gain=33 mV/fC, Peaking Time=4 µsec, respectively. Furthermore, by acting on the channel address (on board connectors Ji) and feeding an input pulse to the correspondent connectors Ji+1, there is the possibility to individually test anyone of the 128 ASICs' channels, one at a time.



Fig. 6-a. Component side view of the ASIC PCB, together with the on-board connectors. The connectors coupling the PCB with the CZT detector output multipin connectors (J1 & J2) are soldered on the opposite side.



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Fig. 6-b. Picture of the ASIC side in the POLCA2 interface board. The pads labelled Tp1, Tp2, Tp3, Tp4 are test points for regulated + 3V (independent checks for outputs provided by four LT1763-3 regulators), while the ones labelled Tp5, Tp6, Tp7, Tp8, TP9 are test points for GND.



#### 3.1. The FE mechanical arrangement

In the original design the FE (CZT detector, ASIC PCB, HV DC-DC converter, Voltage preregulators) should have been included in the same container. However, due to the 3.5 Watt power consumption of the ASIC PCB and the tight proximity with the CZT detector, the system temperature tend to rise up 30-35°C with an ambient kept at about 24°C. Since the rise in detector temperature tends to increase the leakage current, so degrading the overall noise performance, it was decided to separate the ASIC PCB container from the CZT detector box, trying to reduce a tight thermal coupling. This led to the arrangement schematically shown in Fig. 7.



Fig. 7. Mechanical assembly of POLCA2 experiment: three boxes, mechanically and electrically connected, provide EMI protection and thermal insulation of the CZT detector with respect to the other FE subsystems. Lateral view from the higher ASIC PCB dimension. The ASIC PCB dimensions are 10cmx7cm, the dimensions of the containers are 15cmx8cm (height is different for the three boxes).

#### 3.2. The ASIC PCB electrical harness

The ASIC PCB electrical Input connectors and the related functions are listed in Table II. Except for the connectors J1&J2 coupling the CZT detector to the ASIC PCB, all the connectors are card-edge type and are wired on the PCB component side.



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Connector	Function	ASIC #	IC	Notes	Connector Type
J1	Inputs from CZT			Solder Side	100 pin Panasonic
J2	Inputs from CZT			Solder Side	100 pin Panasonic
J3	Ch SEL ASIC # 1	1	<b>U1</b>	<b>Component Side</b>	Molex 5 pin
J4	Pulser In ASIC #1	1	<b>U1</b>	<b>Component Side</b>	Molex 2 pin
JP1	Gain Setting ASIC #1	1	<b>U1</b>	<b>Component Side</b>	Jumper 2 positions
JP2	Peak Time ASIC # 1	1	<b>U1</b>	<b>Component Side</b>	Jumper 2 positions
J5	Ch SEL ASIC # 2	2	<b>U2</b>	<b>Component Side</b>	Molex 5 pin
J6	Pulser In ASIC # 2	2	<b>U2</b>	<b>Component Side</b>	Molex 2 pin
JP3	Gain Setting ASIC # 2	2	U2	<b>Component Side</b>	Jumper 2 positions
JP4	Peak Time ASIC # 2	2	<b>U2</b>	<b>Component Side</b>	Jumper 2 positions
J7	Ch SEL ASIC # 3	3	<b>U4</b>	<b>Component Side</b>	Molex 5 pin
J8	Pulser In ASIC # 3	3	<b>U4</b>	<b>Component Side</b>	Molex 2 pin
JP5	Gain Setting ASIC # 3	3	<b>U4</b>	<b>Component Side</b>	Jumper 2 positions
JP6	Peak Time ASIC # 3	3	U4	<b>Component Side</b>	Jumper 2 positions
J9	Ch SEL ASIC # 4	4	U5	<b>Component Side</b>	Molex 5 pin
J10	Pulser In ASIC # 4	4	U5	<b>Component Side</b>	Molex 2 pin
JP7	Gain Setting ASIC # 4	4	U5	<b>Component Side</b>	Jumper 2 positions
JP8	Peak Time ASIC # 4	4	U5	<b>Component Side</b>	Jumper 2 positions
J11	Ch SEL ASIC # 5	5	U7	<b>Component Side</b>	Molex 5 pin
J12	Pulser In ASIC # 5	5	U7	<b>Component Side</b>	Molex 2 pin
JP9	Gain Setting ASIC # 5	5	U7	<b>Component Side</b>	Jumper 2 positions
JP10	Peak Time ASIC # 5	5	U7	Component Side	Jumper 2 positions
J13	Ch SEL ASIC # 6	6	<b>U8</b>	<b>Component Side</b>	Molex 5 pin
J14	Pulser In ASIC # 6	6	<b>U8</b>	<b>Component Side</b>	Molex 2 pin
JP10	Gain Setting ASIC # 6	6	<b>U8</b>	<b>Component Side</b>	Jumper 2 positions
JP11	Peak Time ASIC # 6	6	<b>U8</b>	<b>Component Side</b>	Jumper 2 positions
J15	Ch SEL ASIC # 7	7	<b>U10</b>	<b>Component Side</b>	Molex 5 pin
J16	Pulser In ASIC #7	7	<b>U10</b>	<b>Component Side</b>	Molex 2 pin
JP13	Gain Setting ASIC #7	7	<b>U10</b>	<b>Component Side</b>	Jumper 2 positions
JP14	Peak Time ASIC # 7	7	U10	<b>Component Side</b>	Jumper 2 positions
JP17	Ch SEL ASIC # 8	8	U11	<b>Component Side</b>	Molex 5 pin
J18	Pulser In ASIC # 8	8	U11	<b>Component Side</b>	Molex 2 pin
JP15	Gain Setting ASIC #8	8	<b>U11</b>	<b>Component Side</b>	Jumper 2 positions
JP16	Peak Time ASIC # 8	8	U11	<b>Component Side</b>	Jumper 2 positions
J19	Power In (+4V)			<b>Component Side</b>	Amphenol 2 pin

#### Table II: ASIC PCB Input connectors.

Any Output connector groups 8 ASIC Channels, for a total of 16 8-pin Molex connectors wired on the four peripheral sides of the ASIC PCB Component surface. The Output connectors are labelled as Out(1-8), Out(9-16),....., Out(113-120), Out(121-128).

Fig. 8 shows the correspondence required to relate any CZT Pixel to the ASIC processing Channel: i.e. CZT(Out-J1&J2)- PixelCZT#- ASIC#- ASICCh#-ChannelOutLabelling



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Fig. 8. Correspondence map between J1-J2 CZT pin function and ASIC user defined channels. Unused CZT outputs are tied to GND to limit the electrical field distortion.



#### 3.3. The electrical diagrams of the FE containers

Simple electronics provide interface with the subsystems mounted in the three containers (Box#1, Box#2, Box#3). They are considered in details.

#### **3.3.1. Electronics inside Box#1**

The electronics wired inside Box#1 simply has to:

- provide low voltage supply to power the EMCO high voltage DC-DC converter;
- provide the output voltage monitor (low-voltage, 0-5V) able to control the HV supply;
- permit the high voltage regulation by action on a potentiometer accessible from the external. The electrical diagram is shown in Fig. 9.



Fig. 9. Components wired inside the Box#1 to give HV Bias to the CZT detector and make possible external control.

The High Voltage monitor value as a function of the High Voltage applied to the CZT detector is given below in Table III. Minimum (-216 V) and maximum (-822 V) high voltage are due to the series resistors in the regulation network. The Imarad CZT typical bias voltage is -600 V.

The sensitivity of the HV monitor is of the order of 4.05 mV(out)/1V(HV).



HV (Volt)	HV Monitor (Volt)
- 216	0.878
- 300	1.219
- 400	1.618
- 500	2.023
- 600	2.430
- 700	2.835
- 800	3.242
- 822	3.332

Table III. The relation between the HV bias voltages and the HV monitor values.

#### 3.3.2. Electronics inside Box#2

No additional electronics is wired inside Box#2, except for the ASIC PCB. The input power connector (+4Volt DC) is J02 and outside remotely protection diode is to be used to prevent from reverse supply polarity. J02 is connected to the on-board 2-pin connector Amphenol J19.

#### **3.3.3. Electronics inside Box#3**

No electronic component is wired inside Box#3, unless the Takes electronics require a reduction in any channel gain. If it is needed to reduce the channel gains, in the Box#3 16 DIP sockets are provided permitting to reduce the overall signal gains by placing in series to any channel a resistor in accordance with the Takes electronics requirements. If no gain reduction is required, jumpers will transfer the ASIC outputs directly to Takes electronics inputs. The Box#3 simply accepts the ASIC outputs from the 16-8-pin organized Molex outputs and adapt them to the standard inputs of the Takes electronics (DB 37 pin).

Fig. 10-a shows the overall wiring schematics relative to the Front-End subsystems.

If required to use the test facility for the ASICs, the Box#3 should be removed and connectors for the channel selection (address) and test pulse placed in the position to test the desired ASIC. Channel selection is simply performed by facing the wanted 4-bit configuration in the appropriate channel selection connector (Molex, 5 pin, 1 for pulser enable, 4 for the channel addressing).

#### **3.3.4.** Power requirements

Two power supplies are required by the FE:

- +12V (connector J01) for the EMCO HV DC-DC converter. The power drain is  $\approx$  15 mA at the power-on, lowering to about 5 mA after the burn-in (3 minutes).
- +4V (connector J02) for the ASIC PCB. The power drain is ≈ 850 mA at the power-on, lowering to about 800 mA after the burn-in (5 minutes).

As power sources a double series regulated-high stability-low ripple/noise laboratory power supplies is used.



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Fig. 10-a. Wiring distribution of the POLCA2 Front-End electronics.



Connector	Function	Туре		
J01	+12V power In (HV)	2-pole Fischer	Box#1	
LB	HV Monitor Out	Mini sockets	Box#1	
J02	+4V power In (ASIC PCB)		Box#2	
1	Out 1-16/In Takes	DB37S	Box#3	Cable + flying connector
2	Out 17-32/In Takes	DB37S	Box#3	Cable + flying connector
3	Out 33-48/In Takes	DB37S	Box#3	Cable + flying connector
4	Out 49-64/In Takes	DB37S	Box#3	Cable + flying connector
5	Out 65-80/In Takes	DB37S	Box#3	Cable + flying connector
6	Out 81-96/In Takes	DB37S	Box#3	Cable + flying connector
7	Out 97-112/In Takes	DB37S	Box#3	Cable + flying connector
8	Out 113-128/In Takes	DB37S	Box#3	Cable + flying connector

Table IV∙ li	st of the I/O	connectors o	of the POI	CA2 FE
1 4010 1 7 . 11	St OI the I/O	connectors o		$\mathcal{O}$



#### Takes INPUT Connector

Fig. 10-b. Correspondence between the physical pins in the Takes connector and the electronics channels in the multi-parametric system.

#### 4. The POLCA2 Read out and Acquisition system

The POLCA2 experiment is represented by the block diagram of Fig. 11. As desribed above (section 2 & 3), the FE detection system and Electronics provide 128 analog signals to the Read-Out Electronics (Takes). Any CZT channel, independently amplified and shaped by active semigaussian filters inside the ASIC to which it is connected, is separately presented to the Takes electronics at an input to which a unique address is associated.



**Coincidence** Logic **Data Conversion** Data Acquisition

Data Handling

1

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Intris

I/O Data Handling

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Fig. 11. The POLCA2 experiment with subsystems set in evidence together with the overall control CPU.

ŏysten

pplic.

I/O card

RS232 Data Acq H/W

NI DAQ 6533

sw

Both the HW and SW have been described in detail (IntRep-Polca1: Ref. d). It should be underlined the main features of the Takes Electronics. Any signal is presented to a peak stretcher (**PPS**) and to a voltage comparator (minimum energy threshold  $E_{min}$ ). The peak voltage of any analog signal overcoming  $\mathbf{E}_{\min}$  is pre-stretched for a time of the order of the input pulse rise time ( $\approx$ 0.7 µsec). For the 128 pixel signals configuration, if within the coincidence window time, selectable among 1, 2, 4, 8, 16  $\mu$ sec, one or two digitized outputs coming from the energy thresholds  $E_{min}$ occur, a post stretching action is issued and the analog data are enabled to be converted in digital by the analog-to-digital converter (ADC). The coincidence criterion is simply based on the fact that single or double events detected within the coincidence time (usually 1 or 2  $\mu$ sec) are accepted as valid and then post-stretched to be converted in digital by the 12 bit flash ADC. The energy of any event (single or double overcoming  $E_{min}$ ) is coded with 10 significant bits and to any channel an address code is associated depending on its physical input wiring. Takes also adds a coded field which allows to detect if a single or double event has occurred within the selected coincidence time.

Takes reserves a word of 32 bit to any single event, two 32 bit pattern for any double event. Furthermore, for design reasons, Takes provides output coded data in serial form.

Since the address associated by Takes to any input does not correspond to the real pixel number (Fig. 3), the POLCA2 SW has to convert the Takes address into the true pixel address in order to reconstruct the square subset read (Fig. 4). The trans-coding is performed by using a look-up table constructed by means of the correspondence listed in Appendix II.

#### 5. The POLCA2 calibration program

The calibration procedure has the main following purposes:

- to inspect for the presence of "dead" pixels;
- $\blacklozenge$  to have quantitative evaluations on the channel-to-channel non-uniformity (pixel efficiency combined with the ASIC channel gain);



- to verify the linearity of the detection system, i.e. the response at various Gamma-ray energies;
- $\diamondsuit$  to evaluate the noise level of each active pixel in order to set the minimum energy threshold;
- to extract the energy resolution of each living pixel at different Gamma-ray energies.

The calibration set-up is shown in Fig. 12 and permits to test any analog channel output provided by the FE electronics by sequentially selecting groups of 8 ASIC channel outputs.



Fig. 11. Calibration set-up to test any individual channel separately.

#### **5.1.1. CZT working ability inspection**

The tests on any CZT pixel have been performed with the basic set-up shown in Fig. 11 by using two <sup>137</sup>Cs and <sup>57</sup>Co radioactive sources which gave the possibility to both inspect for dead/faulty channels and verify the CZT capability to cover the desired energy range [100keV÷1MeV]. The use of a unique external amplification chain and the same stretcher ensures for the inspection on non-uniformities limited only to the CZT-ASIC cannel combination. The ASICs' selected gain is 50 mV/fC and, taking into account the external amplification factor of about 3.5, the detection system permits to cover the desired range, even with an ASIC gain of 100 mV/fC, used with <sup>57</sup>Co. Two totally dead pixel were found over 128 which led to a useful CZT area of about 98.5%. The dead pixels are #172 (amplification channel 46) and #176 (amplification channel 82). As expected, some pixels were found to be more noisy than others and thus almost unusable: typical spectra of a good working pixel and a "poor" one are shown in comparison in Fig. 12.





Fig. 12. Energy spectrum of a good pixel (blue) as compared with that of a noisy pixel (pink), acquired with  ${}^{57}$ Co (above) and  ${}^{137}$ Cs (bottom).

The noisy pixels are the following: channel #39 (pixel# 143), #41 (pixel# 142), #45 (pixel# 154), #46 (pixel# 172), channel #83 (pixel# 192), channel #94 (pixel# 108), channel #118 (pixel# 149).

#### 5.2. Channel-to-channel non-uniformity

By considering the individual pixels' responses at the 122 keV  ${}^{57}$ Co and  ${}^{109}$ Cd energy peak with an ASIC gain of 100 mV/fC, the channel-to-channel non-uniformity has been evaluated by calculating the peak centroid and the deviation from the mean for any pixel (Fig. 13).



Fig. 13. Distribution of the centroid values calculated at 122 keV. The inset reports the statistical parameters of the distribution.

#### 5.3. POLCA2 linearity

Linearity was tested by using <sup>109</sup>Cd (22keV and 88keV), <sup>57</sup>Co (122keV), <sup>137</sup>Cs (662keV) radioactive sources with an ASIC gain of 50 mV/fC (<sup>137</sup>Cs) and 100mV/fC (<sup>109</sup>Cd, <sup>57</sup>Co). The spectra of <sup>57</sup>Co and <sup>109</sup>Cd, obtained irradiating a good pixel, are shown in Fig. 14.

Energy (keV)	0	Centroid Chan	nel	Linear Fit (*)		
	Pixel 121	Pixel 123	Mean Value	а	b	
22	93.73	96.58	95.16			
88	396.64	386.18	391.41	$-3.65 \pm$	$4.490 \pm$	
122	553.59	534.77	544.18	0.10	0.001	
662	733.52	721.66				

(\*) Centroid channel=a+b energy





Fig. 14. a) Energy spectrum of <sup>57</sup>Co (blue) and <sup>109</sup>Cd (red); b) Zoom of the peak at 88 keV.

#### **5.4.** Energy resolution

The same set of data collected for the paragraph 5.4 has been used to calculate the energy resolution of any CZT detection channel (Fig. 15).

#### **5.5.** Threshold evaluation

To better evaluate the low energy threshold, the ASICs' gain has been raised to 200 mV/fC and low peak energies of  $^{57}$ Co were considered.



In Fig. 16 the distribution of the threshold values in channel are shown. The mean value corresponds to about 19.9 keV.



Fig. 15. Distribution of the energy resolutions calculated at 122 keV. The inset reports the statistical parameters of the distribution.



Fig. 16. Distribution of the thresholds values. The inset reports the statistical parameters of the distribution.



#### 5.5. Overall noise evaluation

The measurements have shown that the performance of the POLCA2 detection system is worst than expected from the datasheet of IMARAD (now Orbotech) that, for example, give a resolution of ~5% (FWHM) in average at 122 keV.

The IMARAD value have been obtained with their standard system that use as FEE 2 ASIC's (128 channels each) from IDEAS mounted directly on the backside (anode side) of the detector without employing connectors: from noise level point of view, this configuration is of course better than the POLCA2 one in which the detector is connected to the readout electronics (16 channel eV products ASIC) through three high density connectors and there are longer fan out between the pixel and the input stage of the corresponding ASIC channel.

On other hand the performance of the 16 channels ASIC from eV product have very good noise figure as demonstrated by the performance of 4x4 pixel eV product CZT detector with the same thickness and almost the same pixel pitch of the POLCA2 detection system and the same bias condition: ~3 % (FWHM) at 122 keV, ~8 keV low energy threshold.

Therefore we can infer that the degradation in the spectroscopic performance we observe in the POLCA2 detection system is mainly due to the electrical interface between the detector and the ASIC readout: i.e. increase in parasistic capacitances due to the connectors and the detector fan-out layout.

In order to confirm this hypothesis some more tests will be performed injecting directly in the connectors on the I/F ASIC board known charge pulses corresponding to various energies and evaluating the ASIC output signal FWHM.

## **6.** Conclusions

The functional tests described in this report confirm that the POLCA2 detection system is almost ready to be used for performance tests in different experimental conditions using the TAKES multiparametric back-end electronics to obtain spectroscopic images for single and multiple events.

The POLCA2 will be used as soon as possible in three different experiments:

- Experiment at ESRF (beam line ID15): to evaluate the performance as hard X ray polarimeter of a CZT pixel detector between 100 and 1000 keV.
- Experiment with the X-ray facility at the Ferrara University: to evaluate the response of a CZT pixel detector as a Laue lens focal plane prototype.
- Experiment at the SDof the Leicester University (UK): to assess the performance of an hybrid detector (CCD+pixel CZT detector) as focal plane for coaxial grazing incidence and multilayer mirror for X-ray astronomy (e.g. 0.1/1-100 keV)



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# Appendix I





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# Appendix II

CZT IN	ASIC	I.C.	IN	CZT	Takes IN	Takes IN	Pin
Ch #	#	(	Ch	Pixel #	Ch	Connector	
1	1	U1	1	223	1	1	1
2	1	U1	2	239	2	1	2
3	1	U1	3	238	3	1	3
4	1	U1	4	237	4	1	4
5	1	U1	5	222	5	1	5
6	1	U1	6	221	6	1	6
7	1	U1	7	220	7	1	7
8	1	U1	8	236	8	1	8
9	1	U1	9	219	9	1	9
10	1	U1	10	235	10	1	10
11	1	U1	11	218	11	1	11
12	1	U1	12	234	12	1	12
13	1	U1	13	233	13	1	13
14	1	U1	14	217	14	1	14
15	1	U1	15	232	15	1	15
16	1	U1	16	216	16	1	16
17	2	U2	1	174	17	2	1
18	2	U2	2	190	18	2	2
19	2	U2	3	173	19	2	3
20	2	U2	4	206	20	2	4
21	2	U2	5	189	21	2	5
22	2	U2	6	205	22	2	6
23	2	U2	7	187	23	2	7
24	2	U2	8	188	24	2	8
25	2	U2	9	204	25	2	9
26	2	U2	10	186	26	2	10
27	2	U2	11	185	27	2	11
28	2	U2	12	203	28	2	12
29	2	U2	13	202	29	2	13
30	2	U2	14	201	30	2	14
31	2	U2	15	200	31	2	15
32	2	U2	16	184	32	2	16
33	3	U4	1	159	33	3	1
34	3	U4	2	158	34	3	2
35	3	U4	3	157	35	3	3
36	3	U4	4	175	36	3	4
37	3	U4	5	191	37	3	5
38	3	U4	6	207	38	3	6
39	3	U4	7	143	39	3	7
40	3	U4	8	127	40	3	8
41	3	U4	9	142	41	3	9
42	3	U4	10	126	42	3	10
43	3	U4	11	156	43	3	11
44	3	U4	12	155	44	3	12
45	3	U4	13	154	45	3	13
46	3	U4	14	172	46	3	14

General I/O correspondence: CZT pixels-Takes Electronics Input



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47	3	U4	15	171	47	3	15
48	3	U4	16	152	<b>48</b>	3	16
49	4	U5	1	170	49	4	1
50	4	U5	2	153	50	4	2
51	4	U5	3	120	51	4	3
52	4	U5	4	169	52	4	4
53	4	U5	5	168	53	4	5
54	4	U5	6	141	54	4	6
55	4	U5	7	140	55	4	7
56	4	U5	8	139	56	4	8
57	4	U5	9	123	57	4	9
58	4	U5	10	125	58	4	10
59	4	U5	11	138	59	4	11
60	4	U5	12	122	60	4	12
61	4	U5	13	121	61	4	13
62	4	U5	14	137	62	4	14
63	4	115	15	124	63	4	15
64	4	115	16	136	64	4	16
65	5	U7	1	224	65	5	1
66	5	U7	2	256	66	5	2
67	5	U7	3	255	67	5	3
68	5	U7	3	235	68	5	<u> </u>
60	5	U7	5	254	60	5	
70	5	U7 U7	5	254	70	5	6
70	5	U7 U7	7	253	70	5	7
71	5	U7 U7	/ Q	252	71	5	/ Q
72	5	U7	0	251	72	5	0
73	5	U7 117	9	250	73	5	<u> </u>
74	5	U/	10	249	74	5	10
75	5	U/	11	248	75	5	11
/6	5	U/	12	247	/0	5	12
77	5	U/	13	231	//	5	13
/8	5	U/	14	215	/8	5	14
79	5	U7	15	246	79	5	15
80	5	U7	10	199	80	5	10
81	0	U8	1	160	81	0	1
82	6	U8	2	176	82	0	2
83	6	U8	3	192	83	6	3
84	6	U8	4	208	84	6	4
85	6	U8	5	128	85	0	5
86	6	U8	6	144	86	6	6
87	0	U8	7	112	87	6	7
88	6	U8	8	<u>96</u>	88	6	8
89	6	U8	9	110	89	6	9
90	6	U8	10	94	90	6	10
91	6	U8	11	95	91	6	11
92	6	U8	12	111	92	6	12
93	6	U8	13	109	93	6	13
94	6	U8	14	108	94	6	14
95	6	U8	15	93	95	6	15
96	6	U8	16	92	96	6	16
97	7	U10	1	183	97	7	1
98	7	U10	2	90	<b>98</b>	7	2
99	7	U10	3	119	<b>99</b>	7	3
100	7	U10	4	104	100	7	4



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101	7	U10	5	151	101	7	5
102	7	U10	6	117	102	7	6
103	7	U10	7	103	103	7	7
104	7	U10	8	150	104	7	8
105	7	U10	9	167	105	7	9
106	7	U10	10	133	106	7	10
107	7	U10	11	135	107	7	11
108	7	U10	12	105	108	7	12
109	7	U10	13	107	109	7	13
110	7	U10	14	91	110	7	14
111	7	U10	15	106	111	7	15
112	7	U10	16	101	112	7	16
113	8	U11	1	230	113	8	1
114	8	U11	2	214	114	8	2
115	8	U11	3	245	115	8	3
116	8	U11	4	198	116	8	4
117	8	U11	5	182	117	8	5
118	8	U11	6	149	118	8	6
119	8	U11	7	181	119	8	7
120	8	U11	8	166	120	8	8
121	8	U11	9	165	121	8	9
122	8	U11	10	87	122	8	10
123	8	U11	11	118	123	8	11
124	8	U11	12	88	124	8	12
125	8	U11	13	89	125	8	13
126	8	U11	14	134	126	8	14
127	8	U11	15	102	127	8	15
128	8	U11	16	86	128	8	16