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CHANGE RECORD

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SUMMARY

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INTRODUCTION

The GRID VME board is used to store bars energy information coming from the MCAL-FEE in case of a GRID event, and to retrieve time information from the Burst board, in order to add it to the data collected. This data is then sent to a computer through a VME bus.
The board is also provided with a test input that enables it to be controlled via software and used independently from the MCAL-FEE for debug purposes.
These tests have been performed with the TTL buffers instead of the final LVDS buffers.

REFERENCE DOCUMENTS

1. L. Nicolini, 'Agile MCAL_TE – MCAL front end electrical I/F', 02-2002.
2. M. Trifoglio et al., 'Design report of the Proto MCAL Test Equipment for the Agile Minicalorimeter SEM model', AGILE-ITE-RE-001, Tesre report 336/02, 02-2002.
3. A Bulgarelli et al., "*GRID board for the test equipment of the Minicalorimeter prototype*", AGILE-ITE-TN-008 issue 01, 09-2002
4. RT UML

KEYWORD

PLD Programmable Logical Device
PD Photodiode
VHDL

1. TEST REPORT

In this paragraph are shown the timing diagrams generated by the I/O card on the VME crate in some different cases. The path generated is a consequence of the configuration files selected for the test.
For the definition of test sequence a prelimary analisys is performed for the determination of state chart (see [6]) of the board. From this some test sequences are defined.

1.1 DEFINING TEST SEQUENCE

The state chart is said to be *constructive*. This means that all the behavioural of the object is described with the state chart.
But for the definition test sequence it is important to capture only the main behaviour of the board, starting from the constructive model. What that state diagrams do not show are typical paths through the state space as the system is used. This typical path is called *scenario*. A scenario is said to be a *semi-constructive* model of the object, because within it there aren't enough information to fully define the complete behavioural model.
Based on these concepts it is possible to define the test sequences as a set of scenarios that must be verified.
For this it is important to

- Find the most important behaviour from state diagram
- Select a subset of this behaviour and test it.

1.1.1 SCENARIOS

Only input and output signals and the values of memory and registers are tested. The main output signals that must be verified are:

- T1_START
- T1_YES
- START_CONV
- GSB signals:
  - gsb_stb_dwn
  - gsb_sync_dwn
  - gsb_ck_dwn
  - gsb_data_dwn
- BUSY
- DONE

The scenarios which have been tested so far are the following:

1) real mode (bit1 of configuration register = 1): in this mode it is necessary to test if all the signals are correct. In real mode only the busy mode (bit3 = 0 of configuration register) is tested. The T1_START signal is generated internally because no external equipment is present (bit2=0 of configuration register). The signal timing diagram of Table 2 and Figure 5 in [3] is verified.

2) Test mode (bit1 of configuration register = 0): in this mode it is necessary to test if all the signals are correct. In test mode the busy mode is tested. The T1_START signal is generated internally because no external equipment is present (bit2=0 of configuration register).

Further tests shall include:

3) Real mode with continuous mode and T1_START generated internally
4) Real mode with busy mode and T1_START generated externally
5) Real mode with continuous mode and T1_START generated externally

2. TEST EQUIPMENTS

The following test equipment was used:

1) an oscilloscope HP 54645D
2) a pattern generator HP 1663 CP
3) Host Computer interfaced to the VME crate through to SBS Techonologies BIT3 VME/PCI adapter.

3. TEST SEQUENCE

3.1 SCENARIO 1: REAL MODE

3.1.1 THE CONFIGURATION

For testing purpose an additional test connector is used, showed in the following picture.

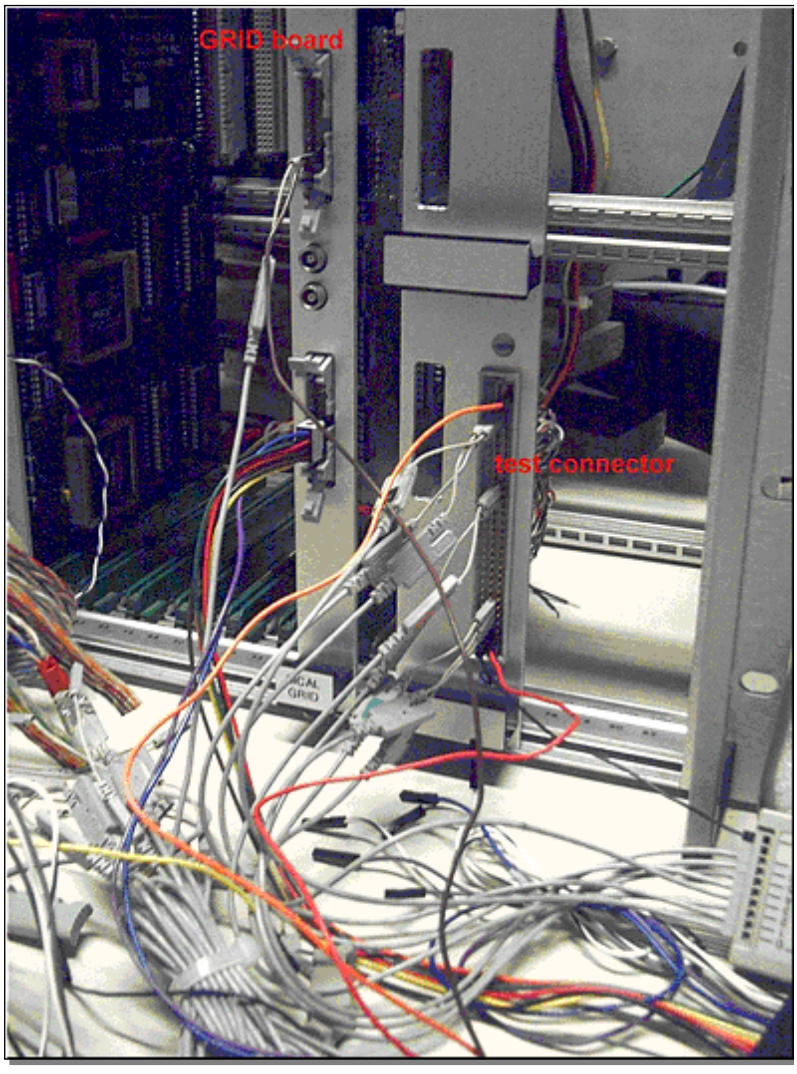

Figure 1:

In the following picture is showed the connections between the GRID board and the Test Equipment.

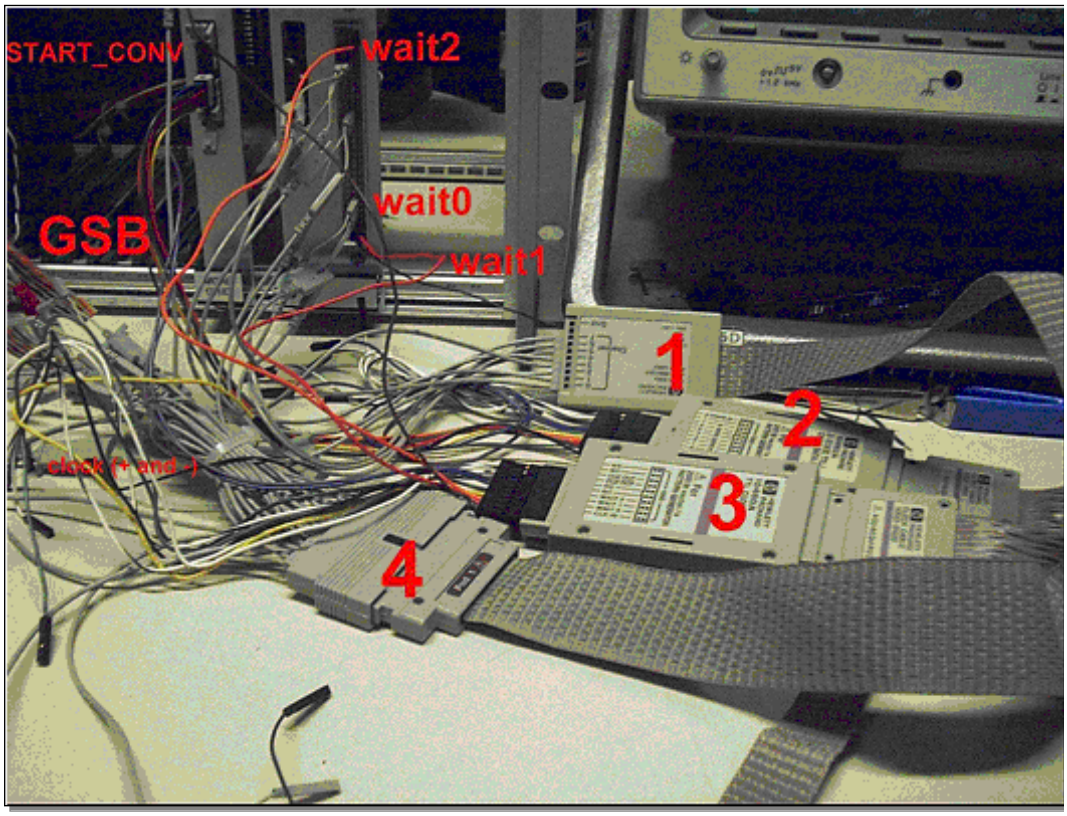

Figura 2:

1. the input pod to the oscilloscope
2. the output signal pod of the pattern generator with GSB signals
3. the clock pod with the clock signal (input for board, showed as *clock (+ and -)*) and with the waits signals as input of the pattern generator
4. the input pod to the pattern generator

The START_CONV+ is an input for pod 3 as wait 0 signal. The START_CONV- is an input for pod4. The wait1 and wait 2 signals are connected to GND pins of the test connector. The wait condition of the pattern generator is set with wait0=1, wait1=0, wait2=0.

3.1.2 THE VALUE ASPECTED

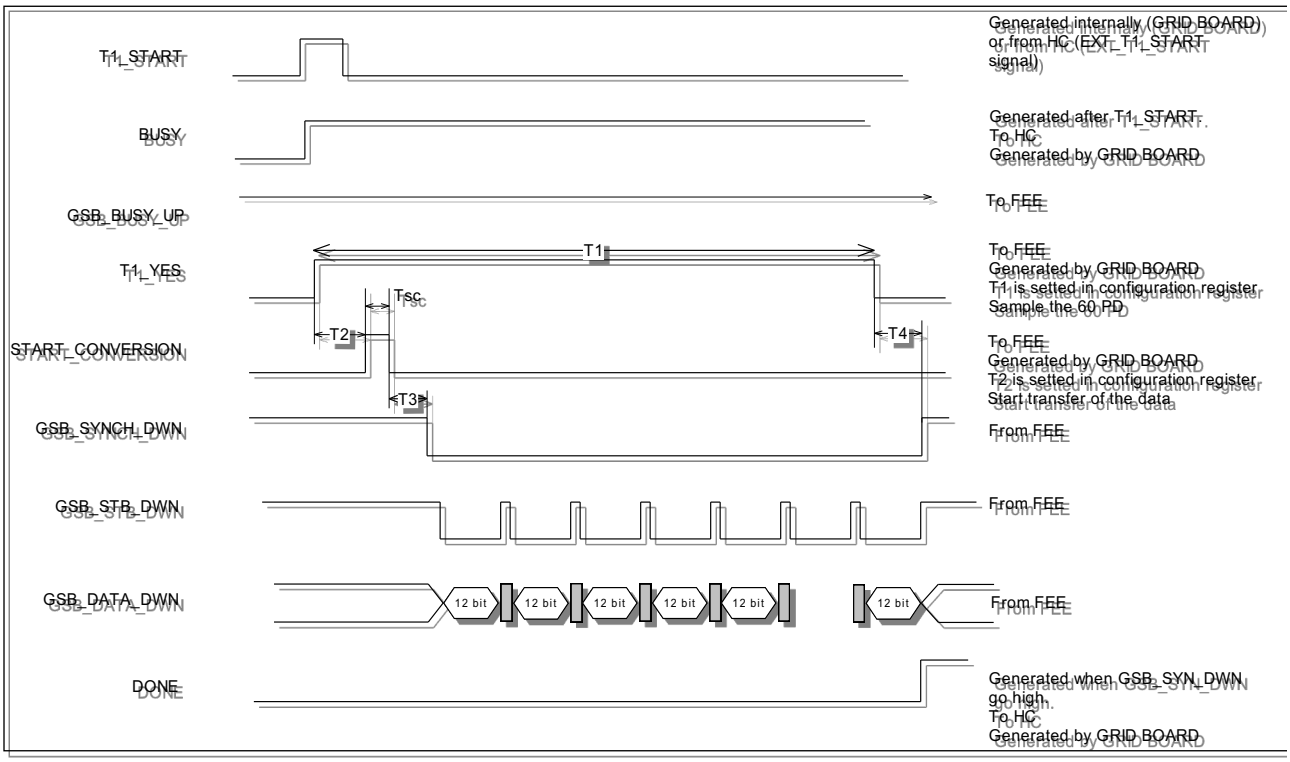

Figura 3: GRID timing diagram

Name	Formula	Min	Max	Description
T1	[0, 255]	0 us	255 us	T1_yes length (programmable)
T2	[0, 255]	0 us	255 us	Start conversion delay (programmable)
T3	[1,4]	1 us	4 us	Data transfer delay
Tsc	200	200 ns	200 ns	Synchronous with ck5 rising edge

Table 1: timing of output signals

3.1.3 THE TESTS

The following timing diagram is generated with the following test equipment:

1) software protoMCALTestboards
2) oscilloscope for reading of the signals
3) pattern generator as input of the board. The data transfer between pattern generator to GRID board starts using the STARTC signal as trigger. The following code is used for the generation of the pattern:

INIT SEQUENCE START

```
INIT SEQUENCE END
MAIN SEQUENCE START
                    010101
                    010101
WAIT A              010101
START LOOP “0”   REPEAT 25 TIMES
                    010101
END LOOP “0”
START LOOP “1”   REPEAT 60 TIMES
                111000
                111000
                101010
                111000
                111000
                101010
                111000
                111000
                101010
                111000
                111000
                101010
                110001
END LOOP “1”
START LOOP “2”   REPEAT 5 TIMES
                010101
END LOOP “2”
                010101
MAIN SEQUENCE END
```

WAIT A = (WAIT 2=0, WAIT1=0, WAIT0=1) con WAIT2 e WAIT1 collegati a GND, WAIT1 collegato a START_CONV

I bit della sequenza corrispondono al SYN (GSB_SYN_DWN), STROBE (GSB_STB_DWN), DATA (GSB_DATA_DWN).

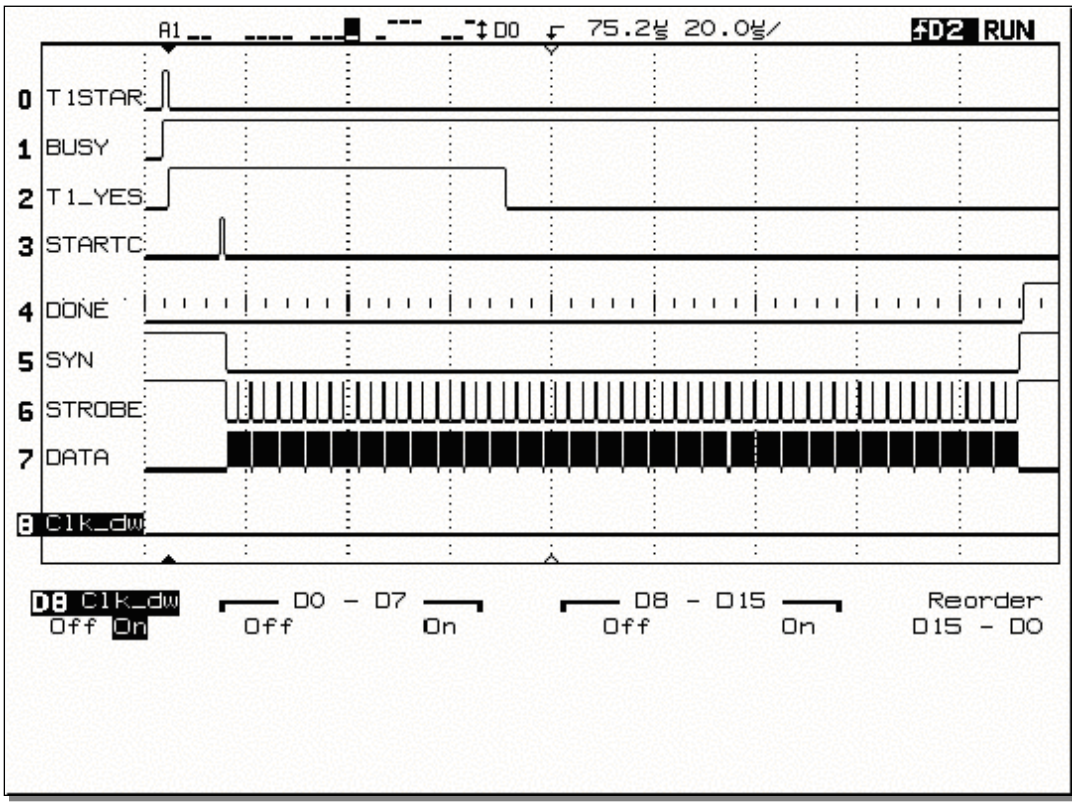

Figure 4:

The configuration register 2 was setted with the value 0x00a in internal mode. After this,

1) a reset signal with the value 0x4053 was generated.
2) Polling on BUSY and DONE signal
3) Internal mode memory and reading of the memory

On the oscilloscope has been verified that the duration of T1 and T2 were correct, but Tsc lasts 1 us (should be 200 ns) (verificare con Laben).

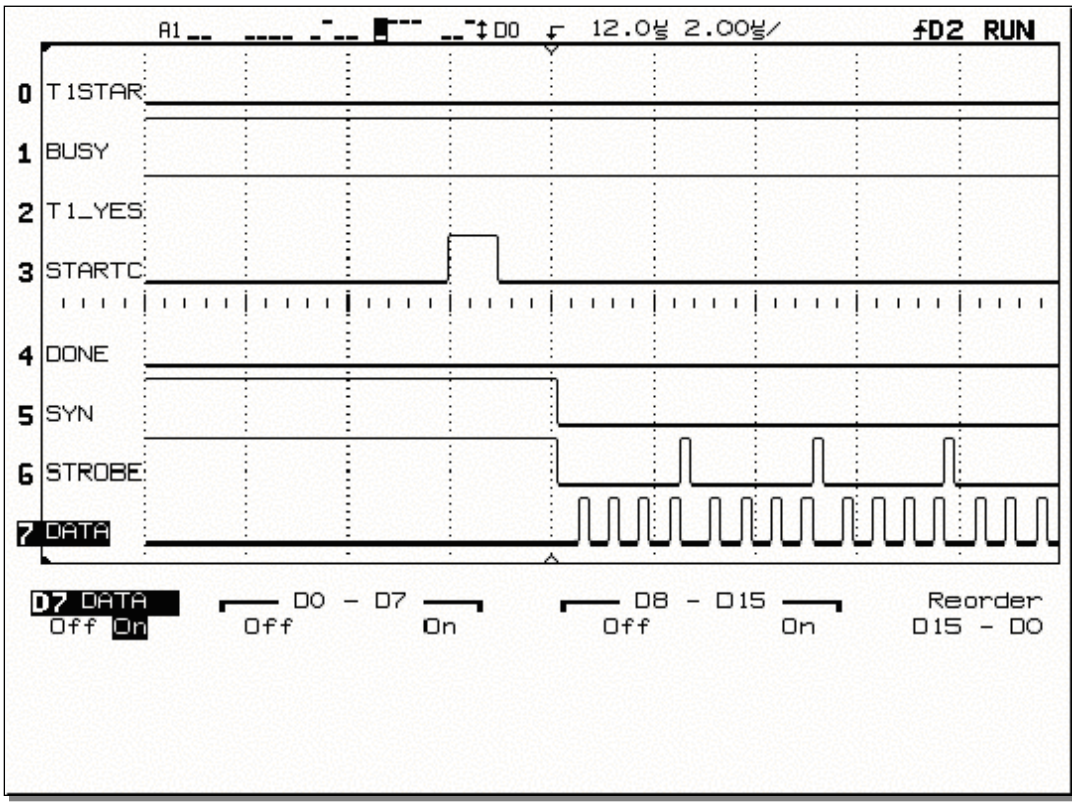

Figura 5:

T3 has been verified at 1 us (see Figure 4) and 4us (see Figura 5).

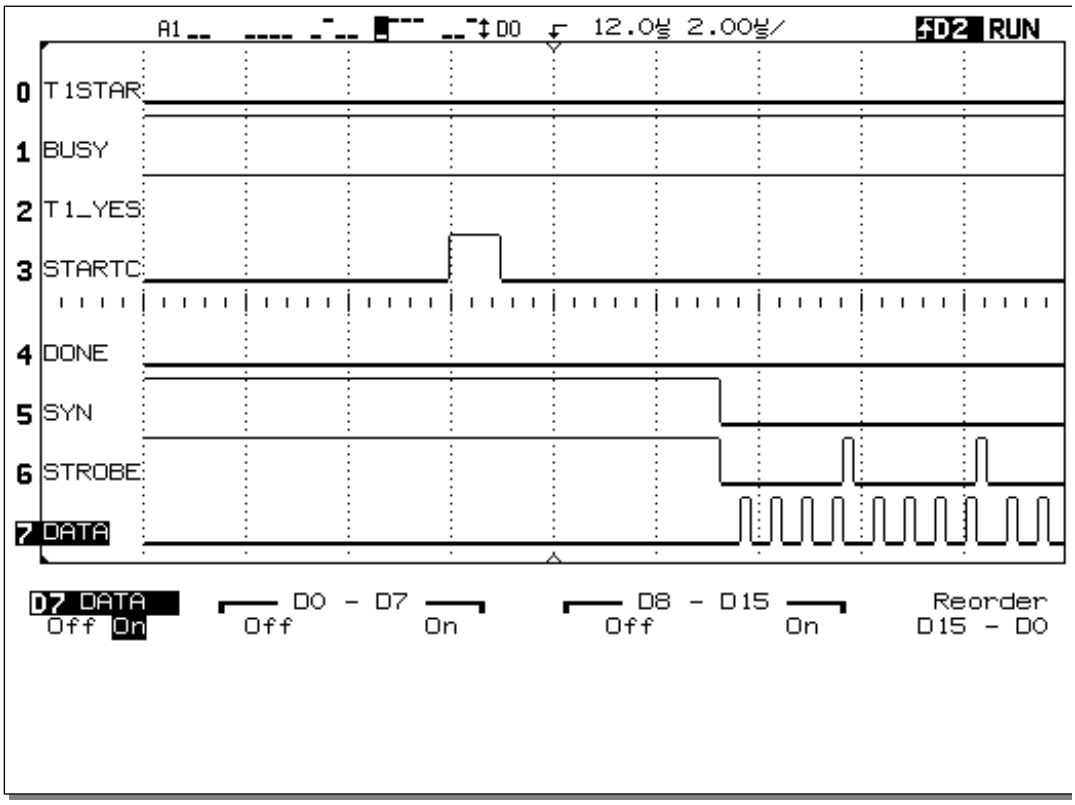

Figure 6:

In both cases the waveform (see Figure 4 and Figure 6 obtained with oscilloscope) and the data read from the GRID board and decoded by the Host Computer were as expected.

3.1.4 THE TESTS ABOUT THE ADDITIONAL OUTPUT SIGNALS

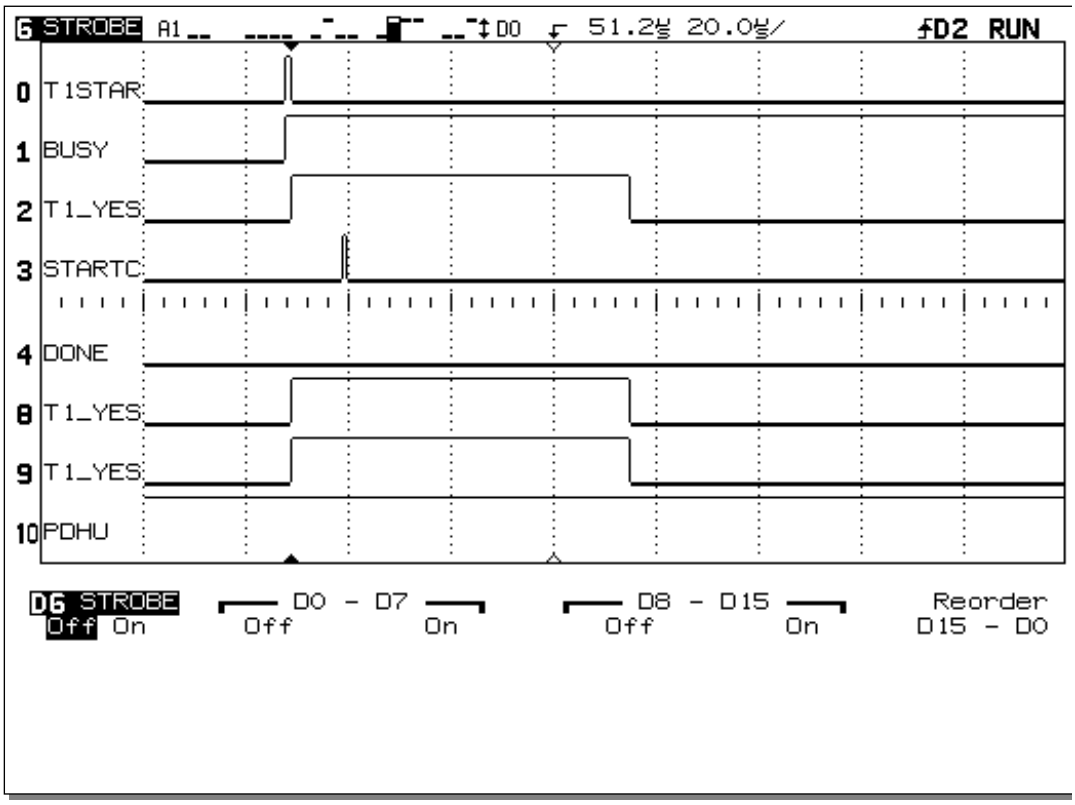

Figura 7:

As shown in Figura 7 the T1_YES 2, T1_YES 3 and PDHU_BUSY signals coming from the output connector (8, 9 and 10) are correct.

3.1.5 THE TIMING SIGNALS

The connection between GRID and BURST board was performed by means of floating cable, as showed in the following picture.

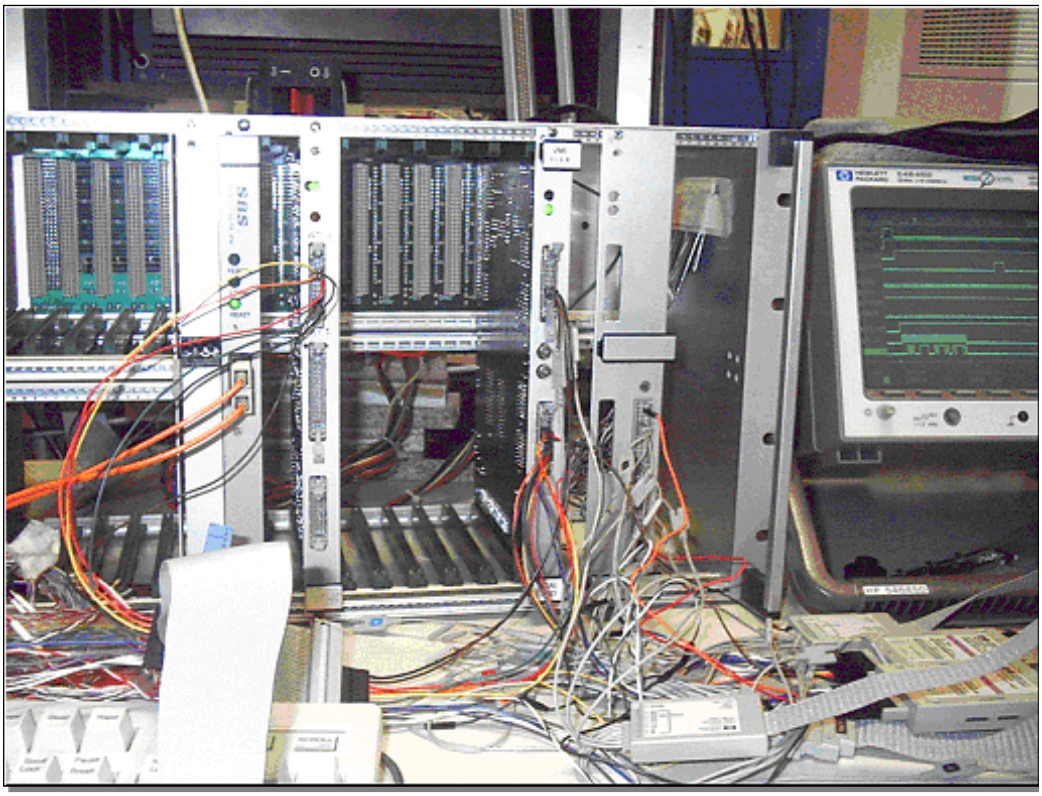

Figura 8:

As shown in the Figura 9 the signals coming from BURST board (9 and 10) are as expected.

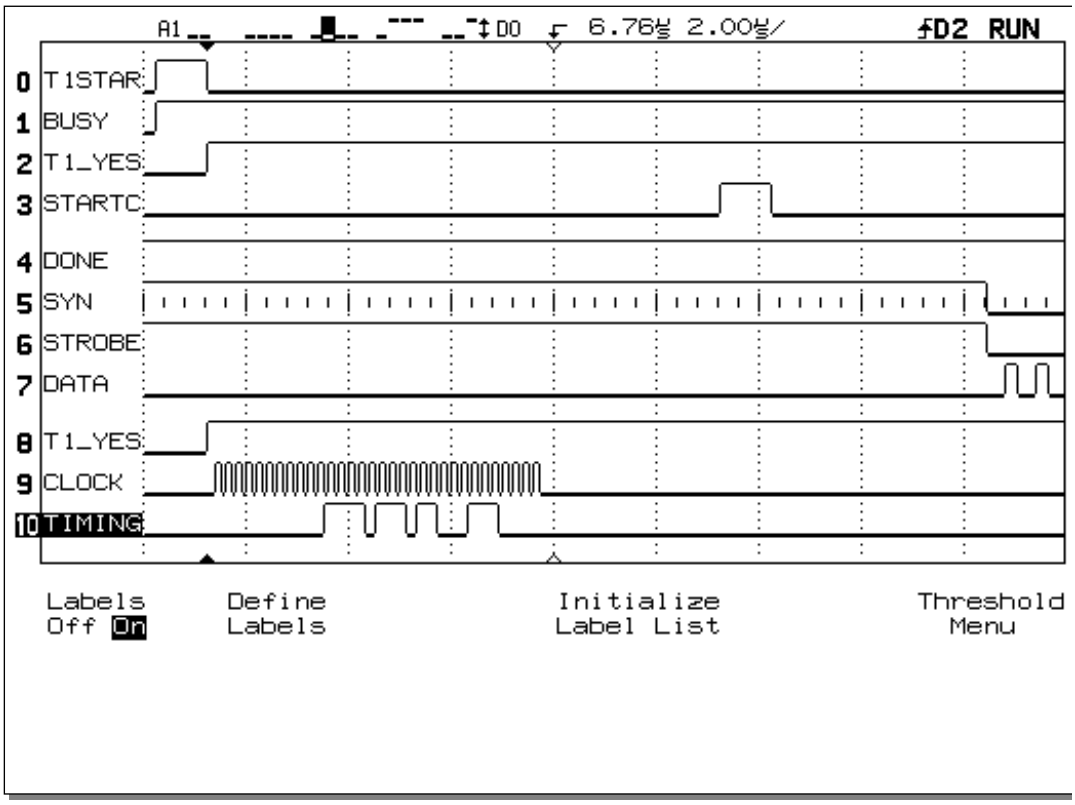

Figura 9:

3.2 TEST SCENARIO 2

Test mode and busy mode.

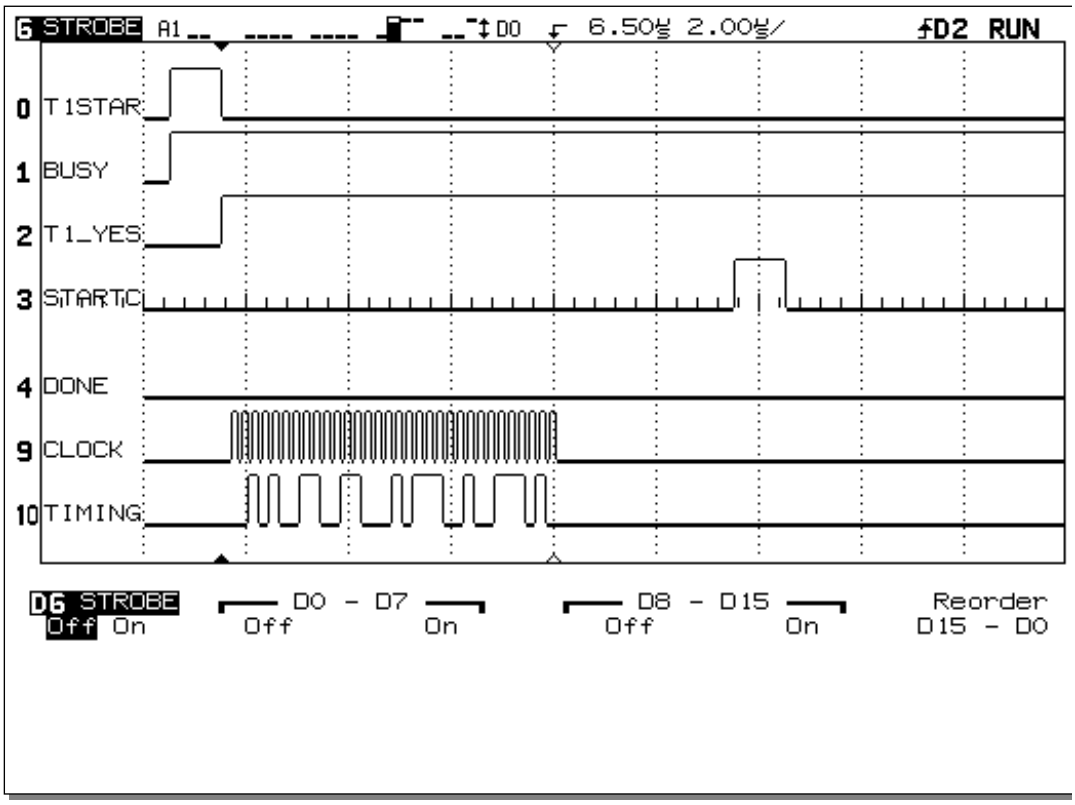

Figura 10:

No data signal can be read, because this signals are not present in the test connector. The data reads from memory are correct and each memory location contains the value 0xf5bc.