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CHANGE RECORD

ISSUE	DATE	PAGE	DESCRIPTION OF CHANGES	RELEASE
0A	22.02.02	All	First issue of the document	1
0B	28.02.02	6	Corrected flow diagram	
		9	Added paragraph 3.4	
		15	Added paragraph 3.11	
		16	Revisited chapter 4	
			Output register renamed to Control register	

SUMMARY

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INTRODUCTION

The Burst VME board is used to store bars energy information coming from the MCAL-FEE in case of a Burst event, and to add time and zombie information to the data collected. This data is then sent to a computer through a VME bus. Moreover it sends time information to the GRID board through a serial line in case that a T1_YES signal is detected.
The board is also provided with a test input that enables it to be controlled via software and used independently from the MCAL-FEE for debug purposes.

Note: In this document the number of bars is considered to be 32, but it seems that it is changing to 30.

REFERENCE DOCUMENTS

1. 'Test equipment for MCAL FEE in BURST mode', T. V. Frøysland, 12-2001.
2. 'Agile MCAL_TE – MCAL front end electrical I/F', L. Nicolini, 02-2002.
3. 'Design report of the Proto MCAL Test Equipment for the Agile Minicalorimeter SEM model', M. Trifoglio et al., AGILE-ITE-RE-001, Tesre report 336/02, 02-2002.

1. BOARD ARCHITECTURE OVERVIEW

A scheme of the board is shown in Figure 1-1. The drawing displays that the board is mainly composed of 3 programmable Altera PLDs:
The first PLD (Data Handling Altera in Figure 1-1) is used to:

- Collect bars energy information for every Burst event from the MCAL-FEE.
- Join bars energy information with time and zombie information for every Burst event and put it in the Event FIFO.
- Retrieve event data from the Event FIFO and send it to the VME bus through a dedicated buffer.

The second PLD (On Board Timing Altera in Figure 1-1) is used to:

- Mark the time of arrival of each Burst event and put it in the Timing FIFO together with the zombie information.
- Mark the time of arrival of each GRID event and send it to the GRID-Board through a serial data line.

The third PLD (On Board VME Interface Altera) is used to manage the interface between the board and the VME bus.

Other components on the board are:

- A 5 MHz clock, used for timing definition.
- 4 connectors:
  - 1 VME connector
  - 2 connectors for communication between the Burst board and the MCAL-FEE or the GRID board (with LVDS signals)
  - 1 connector for test purposes (TTL output).
- 'LVDS to TTL' and 'TTL to LVDS' converters.
- A dedicated buffer that stores the data to be sent over the VME bus.
- Two selectors that specify the base address of the board.

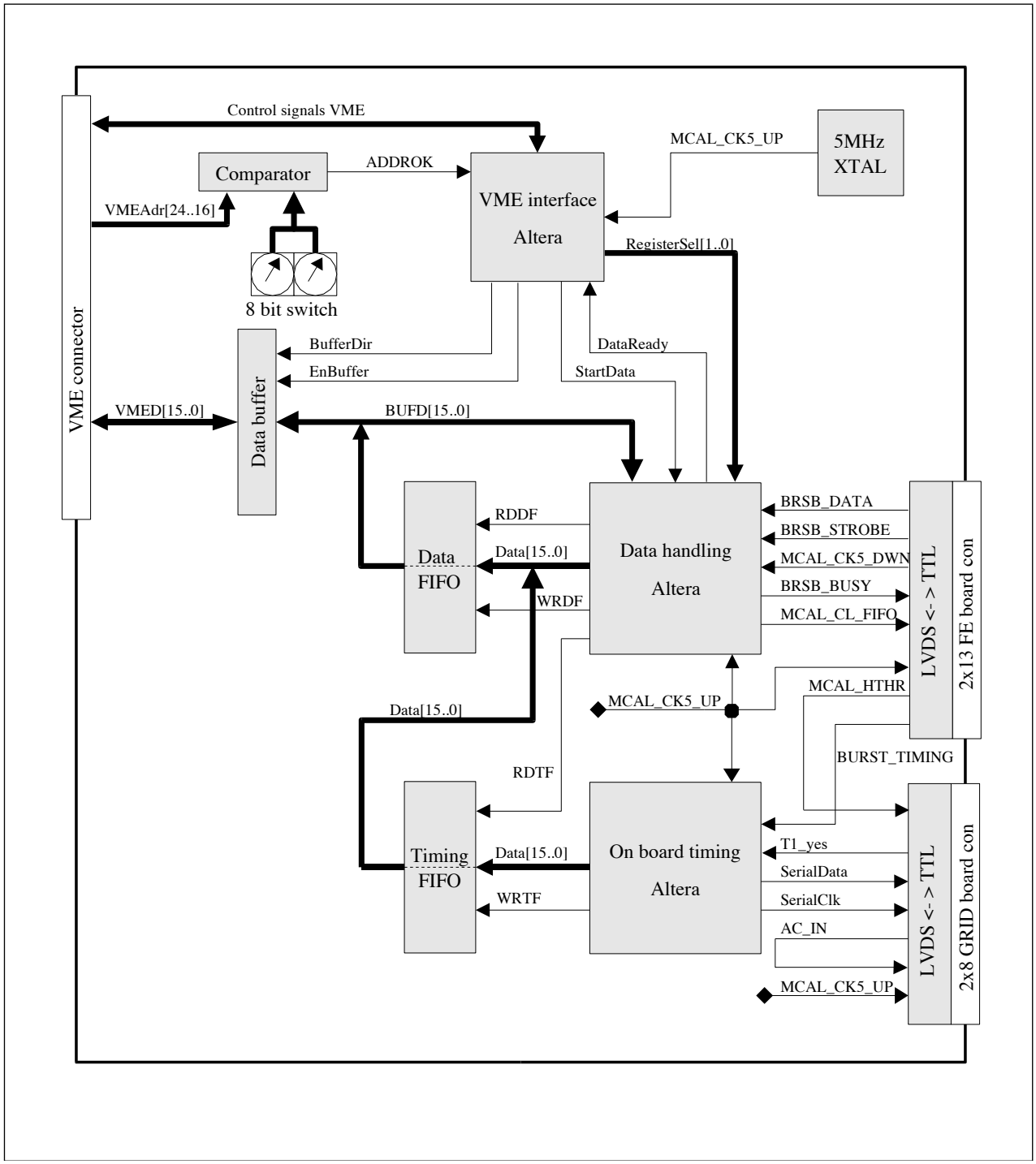


Figure 1-1: Block diagram of the Burst board.

2. FUNCTIONALITY

2.1 STORING BARS ENERGY INFORMATION FOR AN EVENT

When an event is detected on MCAL, the FEE sends data to the Burst board through the BRSB (Burst Scientific Bus). Information on bar address and bar energy is sent to the board as long as the data of all the bars of an event has been transferred (see Figure 3-3).
The data collected from the FEE for an event is joined with timing and zombie information and stored in the Event FIFO (called Data FIFO in Figure 1-1).

2.2 STORING TIME INFORMATION FOR AN EVENT

When a BURST_TIMING signal is detected, timing information is stored in the Timing FIFO together with a zombie flag, that is high if T1_YES signal is high.
The timing information is provided by a 32 bit counter that increase according to the pulses received from an onboard clock with frequency 1.25 MHz and is stored when the BURST_TIMING signal arrives.

2.3 TRANSFERRING TIME INFORMATION TO THE GRID BOARD

In case of a GRID event the time is tagged on the rising edge of the T1_YES signal. The 32 bits of timing data are transferred to the GRID board over a serial line clocked by a signal from the Burst board (SERIAL_CLK) (see Figure 3-2).

2.4 EVENT DATA ACQUISITION

At first the board is initialised by a reset signal that will set the time counter on the board to zero and clears the FIFOs. The board can be reset setting bit 0 in the control register with address 0x08 (see par. 3.10).

The event counter register (address 0x04) contains the number of events stored in the Event FIFO; after initialisation the board makes polling on this register to see if there are events in the FIFO to be read.
When this register is not equal to zero one event should be read from the event FIFO register (address 0x00).
Every time an event is read the event counter decreases by 1, when the event counter gets zero the event FIFO is empty (see).

The FIFO size is 16k words, while the max size of an event is 99 words (3 words for timing information + 32x3 words with bar address and bar energy information, see Table 3-2, 1 word = 16 bit). The FIFO can then contain at least 16000/99≈160 events.

The max time for an acquisition T_{max} is limited by the onboard counter size (2^{32} bits) and by the frequency of the clock (5 MHz / 4) according to the following equation:
$T_{max} = 2^{32}/(1.25 \times 10^6) = 3436$ sec ≅ 57 min
After the counter has reached its maximum value it restarts counting from zero.

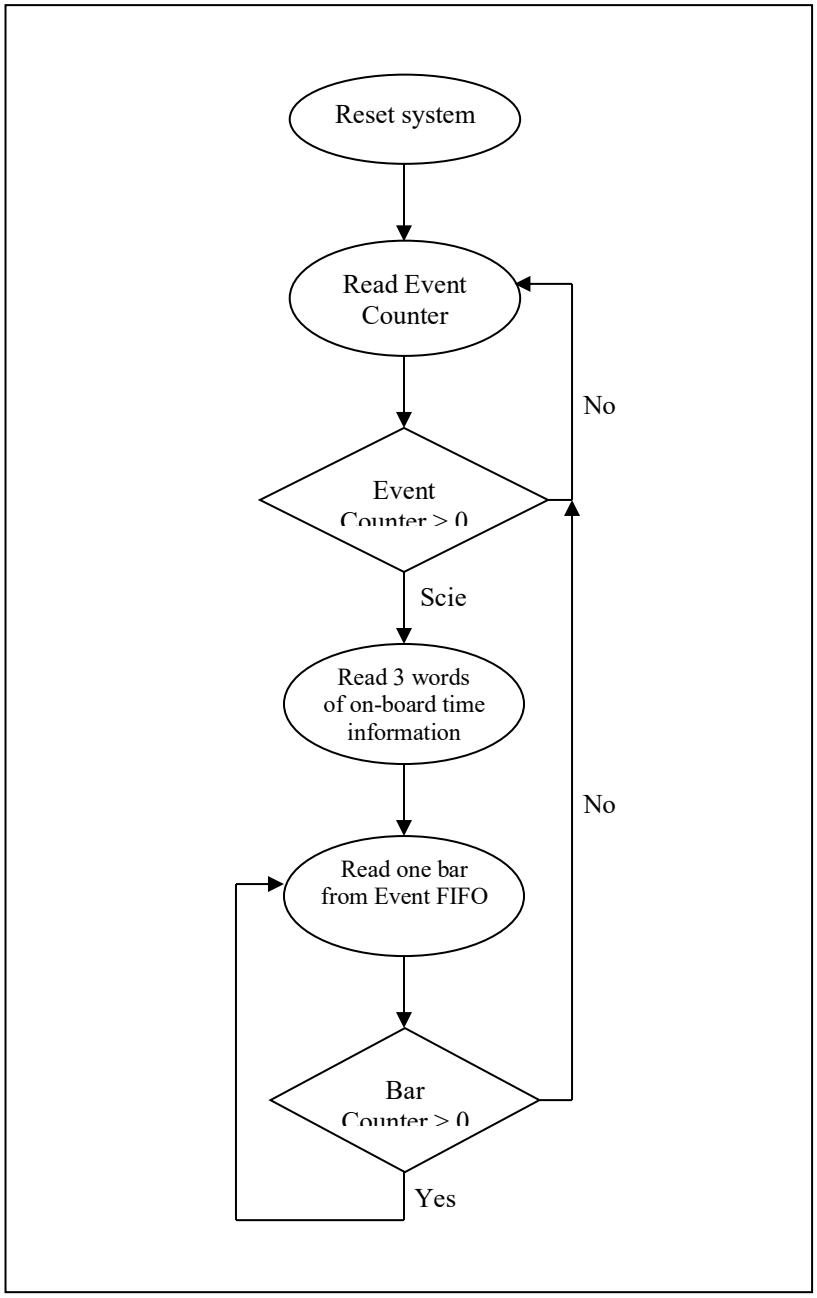


Figure 2-1: Flow diagram of test acquisition sequence.

3. DATA FORMATS AND BOARD INPUT/OUTPUT

3.1 BURST SERIAL BUS DATA FORMAT

Data I/O between the MCAL-FEE and the Burst board is performed over a dedicated bus named BRSB (Burst Serial Bus). When the strobe signal from the FEE becomes low, 17 bits of data are transferred from the FEE to the board.
Two strobe cycles are necessary to transfer a complete set of data, which for every bar is composed of 34 bits and is structured as indicated in the following table.

MSB																LSB
b16	b15	b14	B13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Bar counter (5 bits)					Side A energy (12 bits)											
Bar address (5 bits)					Side B energy (12 bits)											

Table 3-1: Structure of data on the BRSB_DATA_DWN line (34 bits).

BAR COUNTER: 5 bits field.
When a single event is detected this field has value 0.
When a multiple event is detected (one event with multiple bars triggered and the same time tag) this field contains the value 31 at first, and then decreases as the bars data is read. When the data of the last bar is transferred this field jumps to 0.
Example of the Bar Counter for a 5 bars event: 31→30→29→28→0
Example of the Bar Counter for a 3 bars event: 31→30→0
BAR ADDRESS: A 5 bits field that indicates the address of the bar triggered.
SIDE_A/B_ENERGY: 12 bits field, is the digitally converted value of the analogue signal read on each bar's PD (side A and B).

3.2 BURST SERIAL BUS I/O SIGNALS

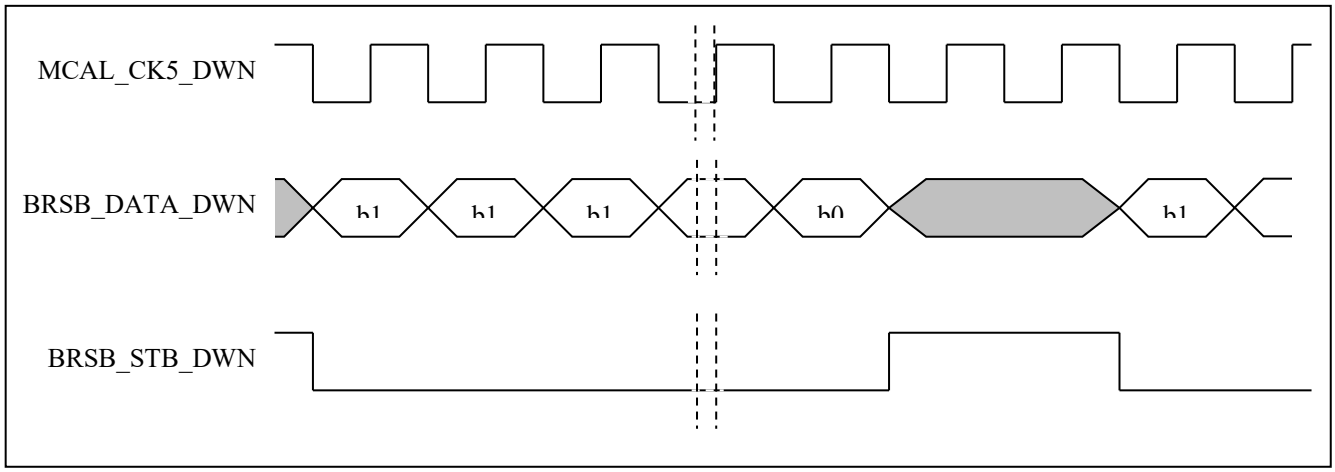
Data I/O between the Burst board and MCAL-FEE are of LVDS type to reduce noise contribution; they have to be converted in TTL signals by dedicated circuits in order to be used on the Burst board.

Follows a list of the INPUT signals to the Burst board from the MCAL-FEE:
MCAL_CK5_DWN 5 MHz Clock from FEE.
BRSB_DATA_DWN BRSB Data Line.
BRSB_STB_DWN BRSB active low strobe that defines a data set of 17 bits.
BURST_TIMING Indicates that a Burst event has occurred, and data is ready to be downloaded from the FEE.

The signals in OUTPUT from the Burst board to the FEE are:

BRSB_BUSY_UP Active low halt for serial transfer from FEE. When it becomes low, the current 34 bit downloading will be finished and no other signal is transferred to the Burst board until the signal stays low (see Figure 3-3).

```
> When the FIFO gets half full the BURST_Busy signal will be set if I
> don't remeber wrong. This means that no more data will be stored
> before some data is read from the FIFO. (Have to check this aswell.)
> I'll give you a better answer on your questions next week.
```



MCAL_CK5_UP 5 MHz Clock to FEE.

Figure 3-1: Timing of the BSRB bus.

3.3 GRID SERIAL BUS I/O

When a T1_YES is detected on the Burst board, time information is transferred to the GRID board over a dedicated serial data line. The time is tagged on the rising edge of the T1_YES signal.
After T1_YES arrival, a serial clock driven by the onboard 5 MHz clock is activated (SerialCLK in Figure 3-2), and 32 bits of timing data start to be transferred to the GRID board over the serial bus.

The signals in OUTPUT from the Burst board to the FEE are:

SerialClk A serial clock that is driven by the 5 MHz onboard clock and is enabled upon arrival of T1_YES signal.

SerialData 32 bits of timing data.

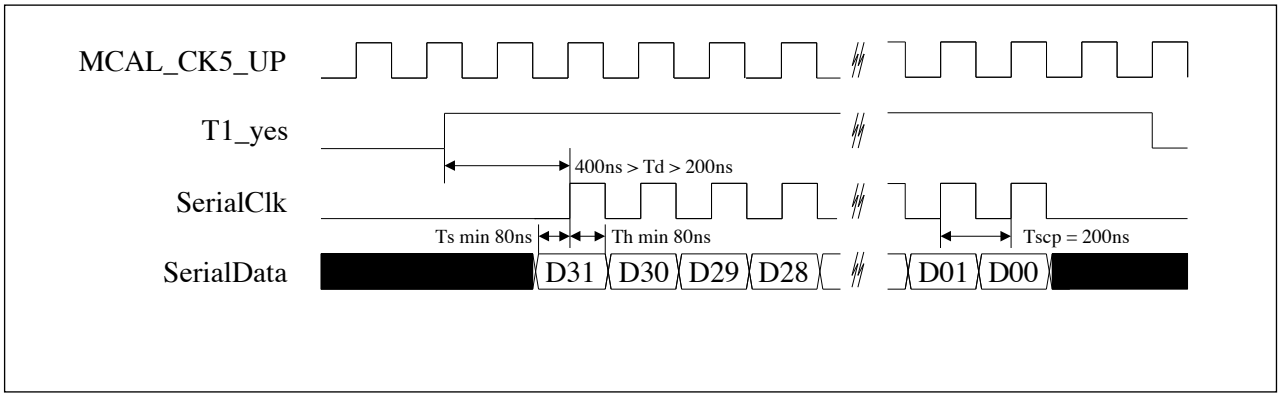


Figure 3-2: Timing of the serial bus to the GRID board.

3.4 VME I/O CARD

For testing purposes, a card is installed in one VME slot. Its function is to get data from the Science Console PC through the VME bus and to translate it in signals FEE-like. These signals are sent as inputs to the Burst board connector 1 (see par. 3.1, 3.2 and Table 3-3).
The card behaves like a Pattern Generator, generating signals that are sent to the Burst board through an Input/Output register.
This card is used when the simulation software is set to External Mode (see par. 4.1).

Bits used in the Input/Output register of the card are:
Bit 0: External Data
Bit 1: External Strobe
Bit 3: External Clock

3.5 FORMAT OF DATA STORED IN THE EVENT FIFO

The data is stored in the event FIFO according to the following table:

MSB															LSB
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
1	NIU						Zom	NIU						2 MSB time	
0	15 bits onboard time														
0	15 LSB onboard time														
0	NIU		Bar Counter					NIU			Bar Address				
0	NIU		Wrd	Side A Energy											
0	NIU		Wrd	Side B Energy											
0	…….														
0															
0	NIU		0	0	0	0	0	NIU			Bar Address				
0	NIU		Wrd	Side A Energy											
0	NIU		Wrd	Side B Energy											

Table 3-2: Structure of one event of data stored in the Event FIFO.

List of terms used in the table:

NIU	Not In Use.
Zom	Zombie bit. Set to 1 if the T1_YES is high when BURST_TIMING goes high.
Bar Counter	This value starts from 31 and counts down for each bar value A and B transferred from the FEE. If the total number of bars hit is < 32 there will be a jump in the counter value, since the last bar will always be recognised by counter value zero.
Bar Address	The address of the following bar value.
wrd	Set to one if the bits transferred for this bar ≠ 17, it means that there is a wrong transfer of data between the Burst board and the FEE.

3.6 ONBOARD DATA HANDLING ALTERA PLD SCHEME

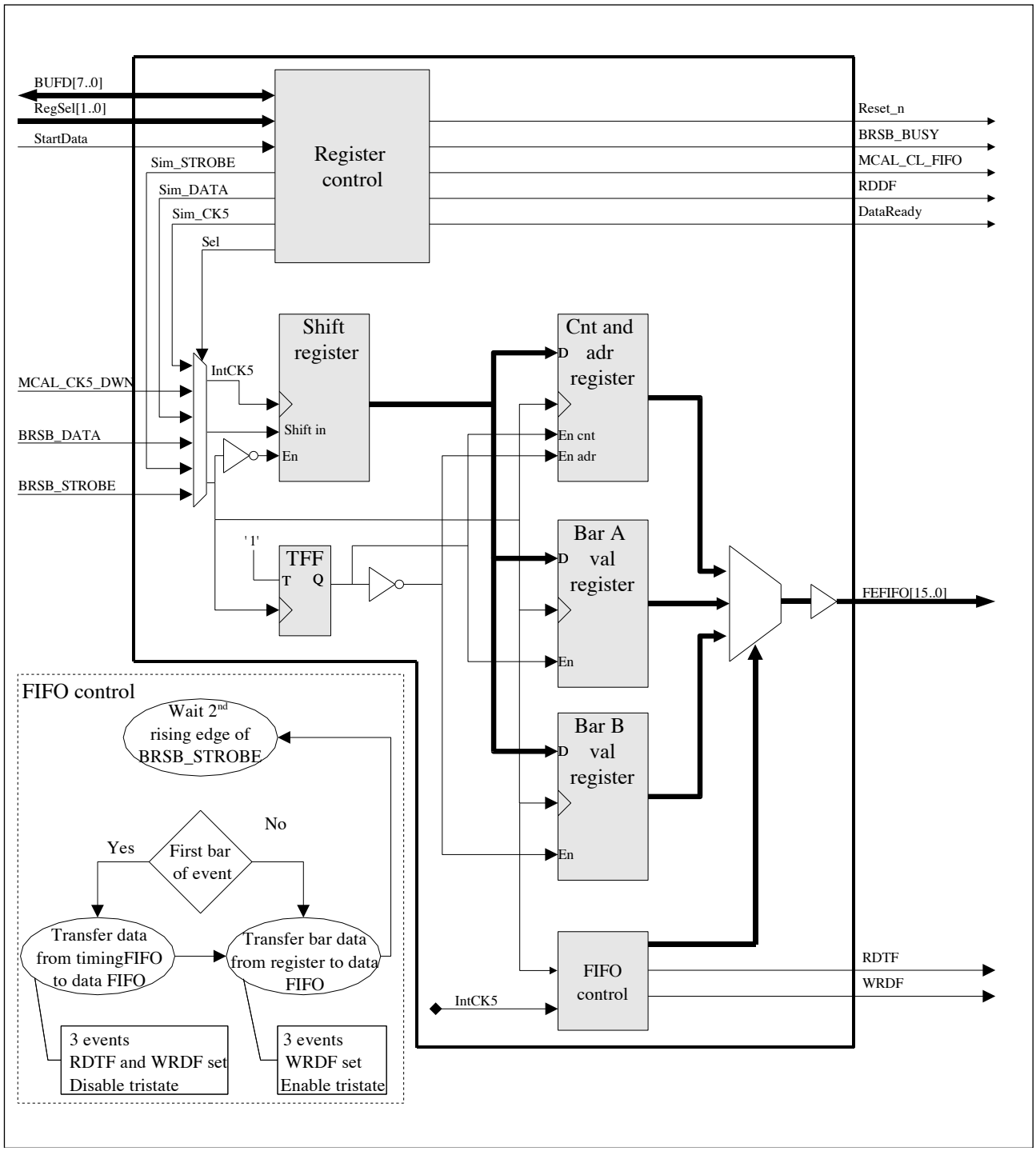


Figure 3-3: Block diagram of the onboard Data Handling Altera PLD, with flow diagram of data acquisition sequence from MCAL-FEE to event FIFO.

3.7 ONBOARD TIMING ALTERA PLD SCHEME

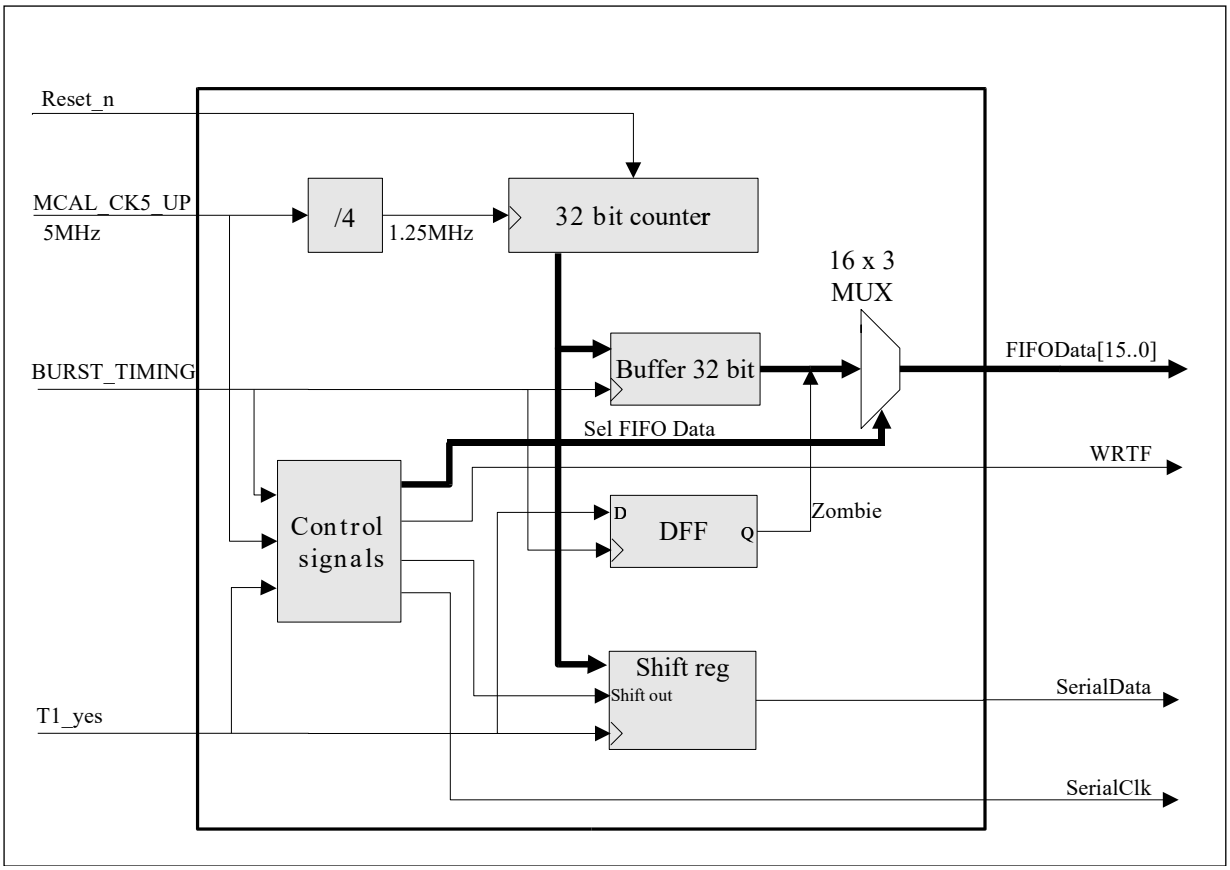


Figure 3-4: Block diagram of onboard Timing Altera PLD.

3.8 CONNECTORS PIN FUNCTION

MCAL Burst Board exchanges signals with the MCAL-FEE through the 2 connectors listed below:

Connector 1 (26 PIN) IDC2X13 TO/FROM FRONTEND	Pol.	PIN	DIR	Description
BRSB_BUSY_UP	+	1	OUT	Burst Serial Bus: Active Low Halt for Serial Transfer to FEE
	-	2		
MCAL_CK5_UP	+	3	OUT	5 MHz Clock to FEE
	-	4		
MCAL_CL_FIFO	+	5	OUT	Clear FIFO on the FEE
	-	6		
MCAL_AC	+	7	OUT	Anticoincidence signal output to FEE
	-	8		
BRSB_DATA_DW	+	11	IN	Burst Serial Bus: Data Line
	-	12		
BRSB_STB_DW	+	13	IN	Burst Serial Bus: Active Low Strobe
	-	14		
BURST_TIMING	+	15	IN	Timing Line for Burst Event
	-	16		
MCAL_CK5_DWN	+	17	IN	5 MHz Clock from FEE
	-	18		
MCAL_HTHR (NIU)	+	19	IN	Fast Trigger (High Threshold)
	-	20		
MCAL_SP_IN	+	21	IN	Spare Input
	-	22		

Table 3-3: Connector 1, 26 pin, signals to/from Front-End.

Connector 2 (16 PIN) IDC2X8 TO/FROM GRID/TRIGGER	Pol.	PIN	DIR	Description
T1_YES	+	1	IN	For Hold and Reset
	-	2		
AC_IN	+	3	IN	Anticoincidence Sign., Logic Network on AC_DFE Board in PDHU Box
	-	4		
MCAL_CK5_UP	+	9	OUT	5 MHz Clock to FEE
	-	10		
TIMING_DATA	+	11	OUT	Timing Data to GRID Board Through Serial Line
	-	12		
SERIAL_CLK	+	13	OUT	Clock to GRID Board Through Serial Line
	-	14		
MCAL_HTH_GRD	+	15	OUT	Fast Trigger (High Threshold)
	-	16		

Table 3-4: Connector 2, 16 pin, signals to/from GRID/trigger.

A third connector is for testing purpose and is used to monitor the signals on the board.

Connector 3 (16 PIN) IDC2X8 TEST CONNECTOR	PIN	DIR	Description
BRSB_DATA_DW	1	OUT	Burst Serial Bus: Data Line
BRSB_STB_DW	2	OUT	Burst Serial Bus: Active Low Strobe
BURST_TIMING	3	OUT	Timing Line for Burst Event
MCAL_CK5_DWN	4	OUT	5 MHz Clock from FEE
MCAL_HTHR	5	OUT	Fast Trigger (High Threshold)
MCAL_SP_IN1	6	OUT	Spare Input
T1_YES	7	OUT	For Hold and Reset
AC_IN	8	OUT	Anticoincidence Sign., Logic Network on AC_DFE Board in PDHU Box
BRSB_BUSY_UP	9	OUT	Burst Serial Bus: Active Low Halt for Serial Transfer to FEE
MCAL_CL_FIFO_N	10	OUT	Clear FIFO on the FEE
DATATOFIFO	11	OUT	
STROBETOFIFO_N	12	OUT	
CLKTOFIFO	10	OUT	
MCAL_CK5_UP	14	OUT	5 MHz Clock to FEE
TIMING_DATA	15	OUT	Timing Data to GRID Board Through Serial Line
MCAL_HTHR	16	OUT	Fast Trigger (High Threshold)

Table 3-5: Connector 3, 16 pin, test connector.

3.9 ELECTRICAL SCHEMES OF THE BOARD

The electrical schemes and the PCB scheme of the Burst board are enclosed to this document. See enclosures 1 and 2.

3.10 **BOARD REGISTERS**

The board uses 24-bit address and transfers 16 bits of data. The base address of the board is in the form:
0xAB00
Where: A=SW2 position
B=SW1 position
The address of the board can be changed acting on the two switches above-mentioned.

There are three registers on the board:

FIFO register:
Base address + 0x00. Read only.
This register is used to read data from the Event FIFO. This register should be read only when the event counter is greater than zero. The MSB signalises the beginning of an event package.

Event Counter register:
Base address + 0x04. Read only.
This register tells the number of events in the Event FIFO. If this register is greater than zero the Event FIFO should be read. It's possible to poll on this register.

Control register:
Base address + 0x08. Read/write.
Bit 0: Write only. Software reset. Resets the board when writing 1.
Bit 1: Write only. MCAL_CL_FIFO. Clears the FEE FIFO.
Bit 3: Read/write. Blocks readout of data from the FEE if 1, normally set to 0.
Bit 4: Write only. Internal Clock. }
Bit 5: Write only. Internal Strobe. } Used to simulate FEE with Burst board only.
Bit 6: Write only. Internal Data. }
Bit 7: Write only. Select mux bit. Set to 1 = internal (VME).
Set to 0 = external (FEE).
If set to 1 the board simulates the FEE signals.

```
For the event counter I
> think it is 8 bit. (Have to check it.) I can make it 16 bit instead.
```

For timing diagrams of the registers see enclosure 3.

3.11 SYSTEM OVERVIEW

Below is shown an image of the VME crate with the Burst board and the I/O card installed. PLDs and connectors position is indicated. The cable that connects the two boards is also visible.

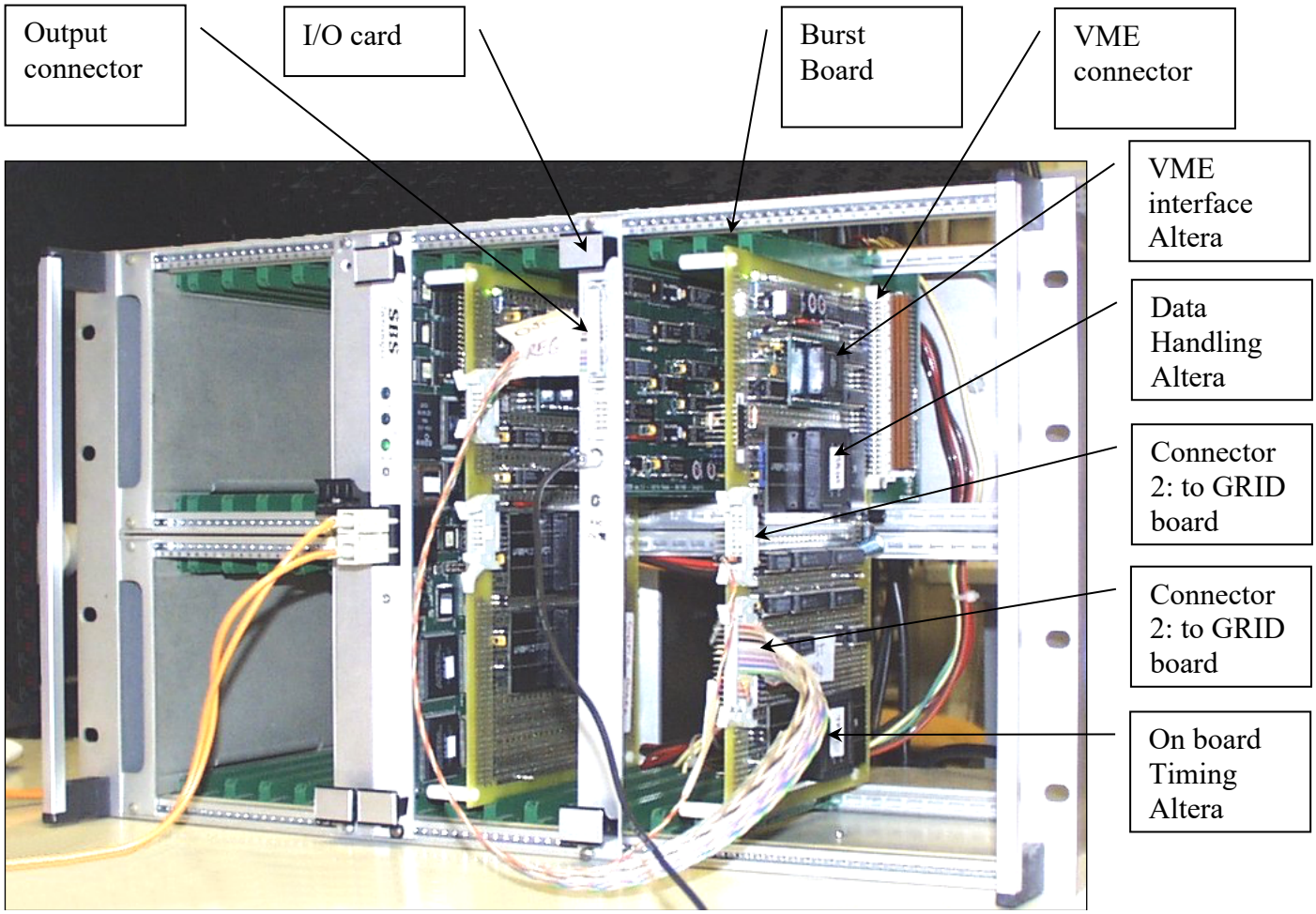


Figure 3-5: Image of the VME Crate with the Burst board and the I/O card installed.

4. SOFTWARE AUTO-CHECK

The software function is to simulate the data sent over the BRSB by the MCAL-FEE, and to verify that all the FIFO reading/writing operations are performed correctly by the onboard PLDs.
Data can be provided to the Burst board by running the software in two different modes:
- External mode
- Internal mode

To switch between the two modes the user must set the bit 7 of the Control Register (see par. 3.10).
In external mode (default) data is provided to the Burst Board through the FEE Connector (connector 1, Table 3-3).
In Internal mode data is provided to the Burst Board over the VME Bus, and signals are generated internally on the board.
Hardware configuration for both the modes of operation in shown in Figure 4-1.

Data is written to the Burst board according to the contents of the configuration file (see par. 4.4), that can contain many events, with single or multiple bars triggered for each event. Otherwise it is possible to define in the front panel of the SW, a single bar event bypassing the configuration file.

Software can run in two different ways:

Single mode	The data contained in the configuration file (or defined in the SW front panel) is sent to the board once, and then read back.
Loop mode	The data contained in the configuration file (or defined in the SW front panel) is sent to the board and is read back continuously until a break is given.

Data is then read by the Science Console from the board over the VME bus and the correspondence of the ‘data sent’ vs ‘data read’ is verified (see Figure 4-6). If such correspondence fails a warning message appears on the screen indicating the details of the mismatch between the two data sets.

4.1 EXTERNAL MODE

Data is sent over the VME bus from the Science Console PC to an Input/Output VME Card (see par. 3.4). The card behaves like a pattern generator, generating signals FEE-like that are sent to the connector 1 of the Burst board.

To simulate the data sent from the FEE to the Burst board, the following signals are generated by the VME card:

BRSB_DATA_DW	Is built according to the information written in the **configuration file** (see par. 4.4), that contains a user defined number of custom-made events.
MCAL_CK5_DWN	Is generated according to the BRSB_DATA_DW signal in order to have the correct data transmission.
BRSB_STB_DW	Is generated according to the BRSB_DATA_DW signal in order to have the correct data transmission.
The BURST_TIMING	Is sent to the board to produce event timing information.
T1_YES	Is sent to the board to produce Zombie flag information.

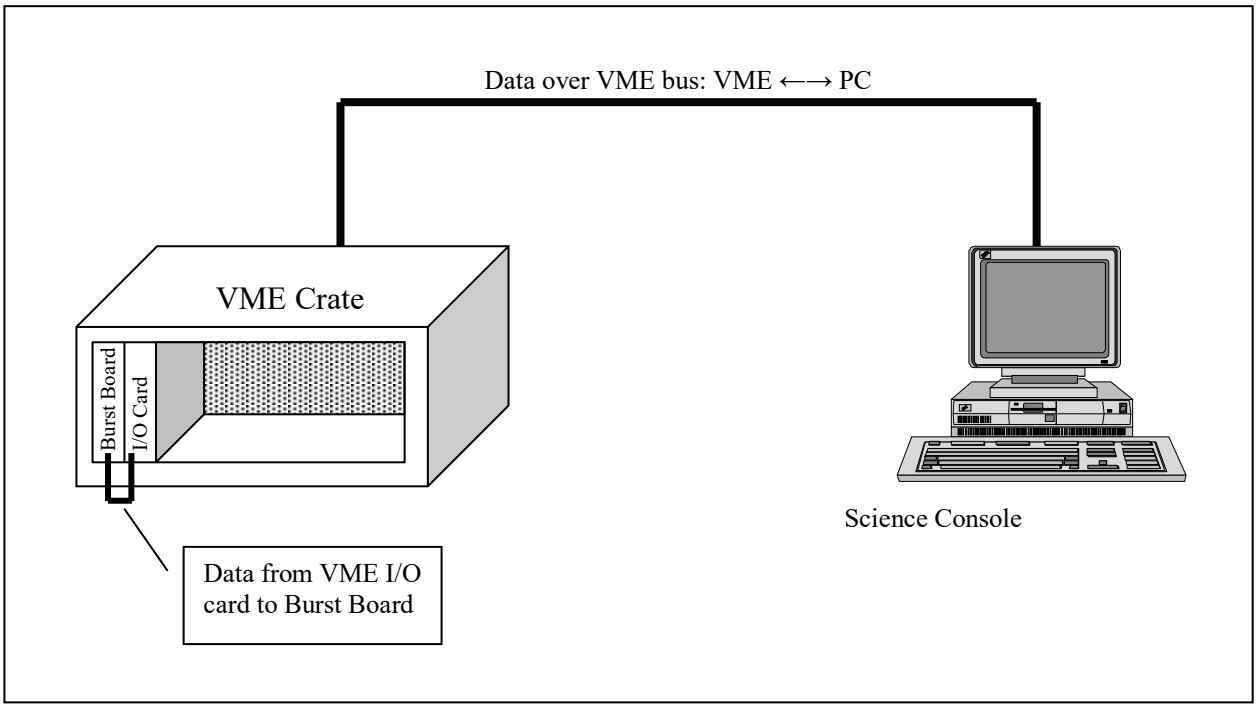
Signals are sent to the Burst board through the VME card. The acquired data is written on the onboard event FIFO.
Data is then read by the Science Console from the board over the VME bus and the correspondence of the two data sets is checked (see Figure 4-6). If such correspondence fails a warning message appears on the screen indicating the details of the mismatch between the two data sets.

4.2 INTERNAL MODE

In internal mode data is sent to the Burst board over the VME bus. Data to be sent is read from the configuration file (see par. 4.4).
The data coming to the board from the bus is collected in a buffer, and then is written it in the bits 4, 5 and 6 of the Control Register.
From the Control Register data is then sent to the Event FIFO, where is stored together with timing information.
In this case NO BURST_TRIGGER signal is sent to the Burst board, so the timing information stored in the Event FIFO always corresponds to 0.

The following signals are generated inside the Burst board:

SIM_CK5	Simulated clock signal
SIM_STROBE	Simulated strobe signal
SIM_DATA	Simulated data built according to the information written in the **configuration file**.



Signals generated from the board are stored on the on board event FIFO.

Figure 4-1: Software auto-check: hardware configuration.

4.3 USING THE SOFTWARE

To launch the software go to the program directory and type *./mcal_test.tcl* ↵. The main window appears (Figure 4-2), here the user has to select the button *BURST TEST* to start the auto-check routine.
A new window appears, that enables the user to perform three kind of test:

- Simulate one bar info.
- Simulate reading configuration data from file.
- Simulate reading configuration data from file with no reading back of the data.

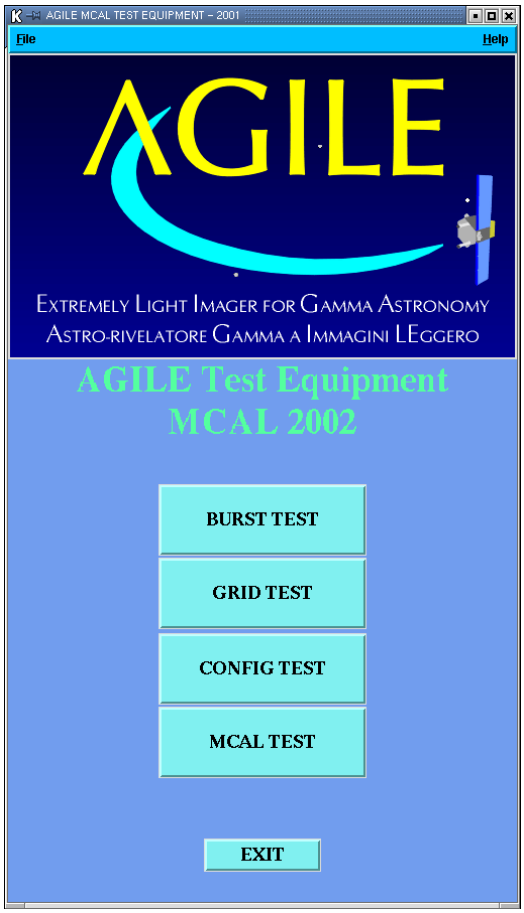


Figure 4-2: Software main window.

4.3.1 SIMULATE 1 BAR INFO

In this mode (Figure 4-3) the user sends to the Burst board data corresponding to a single event. Data is not read back from the board.

Window description:

- Field *Word Info 1* requests the bar counter (00 because this is a single event) and the Bar 1 side A energy value.
- Field *Word Info 2* requests the bar address and the Bar 1 side B energy value.

- Field *From VME(0), I/O(1)* requests the user to write 0 to operate the board in Internal mode, 1 to operate in External mode.
- Button GO LOOP enables the software to operate in Loop mode.
- Button DEBUG enables the software debug mode, that writes details about the read/write procedure while it is being performed.
- Button GO starts the sequence.

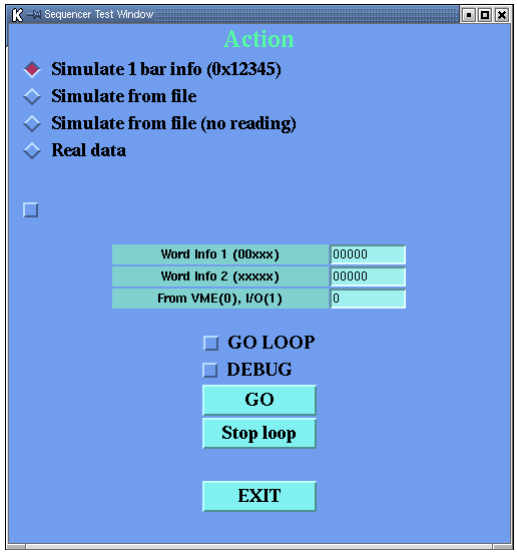


Figure 4-3: *'Simulate 1 bar info'* window.

4.3.2 SIMULATE READING CONFIGURATION DATA FROM FILE

In this mode (Figure 4-4) user sends to the Burst board data corresponding to events written in the configuration file (see par. 4.4). These can be single or multiple events, and there is no limit to the number of events the software can send.
All the data must be sent to the board in order to start the read process from the on board Event FIFO to the Personal Computer memory.

Window description:
- Field *Filename* requests the user to input the name of the configuration file.
- Field *From VME(0), I/O(1)* requests the user to write 0 to operate the board in Internal mode, 1 to operate in External mode.
- Field *T1_yes* requests the user to input the T1_yes bit status.
- Button GO LOOP enables the software to operate in Loop mode.
- Button DEBUG enables the software debug mode, that writes details about the read/write procedure while it is being performed.
- Button GO starts the sequence.

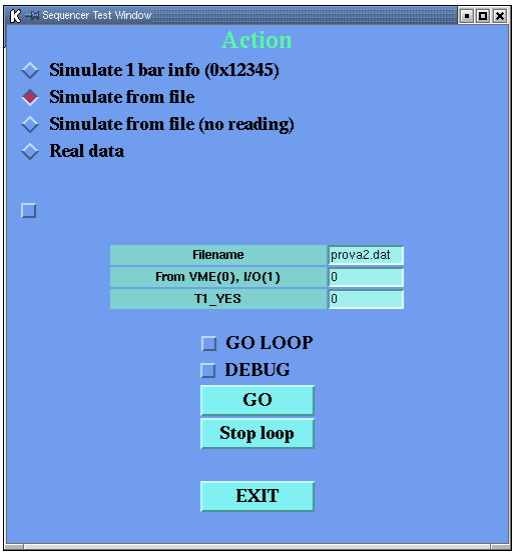


Figure 4-4: *'Simulate from file'* window.

4.3.3 SIMULATE READING CONFIGURATION DATA FROM FILE WITH NO READING BACK OF THE DATA

In this mode (Figure 4-5) user sends to the Burst board data corresponding to events written in the configuration file (see par. 4.4). These can be single or multiple events, and there is no limit to the number of events the software can send.
No reading of data from the Burst board is performed in this mode.

Window description:
- Field *Filename* requests the user to input the name of the configuration file.
- Field *From VME(0), I/O(1)* requests the user to write 0 to operate the board in Internal mode, 1 to operate in External mode.
- Field *T1_yes* requests the user to input the T1_yes bit status.
- Button GO LOOP enables the software to operate in Loop mode.
- Button DEBUG enables the software debug mode, that writes details about the read/write procedure while it is being performed.
- Button GO starts the sequence.

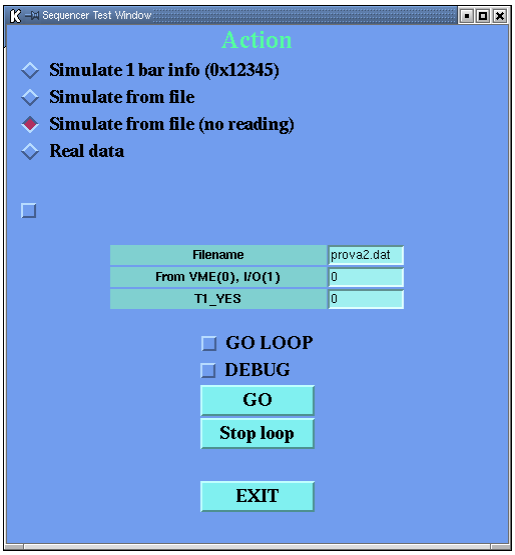


Figure 4-5: 'Simulate from file (no reading)' window.

4.4 THE CONFIGURATION FILE

The configuration file contains data to be sent to the Burst board. Data on the file has the same format used by the FEE to send its data to the board (see par. 3.1). File must be saved in text format in the program directory.

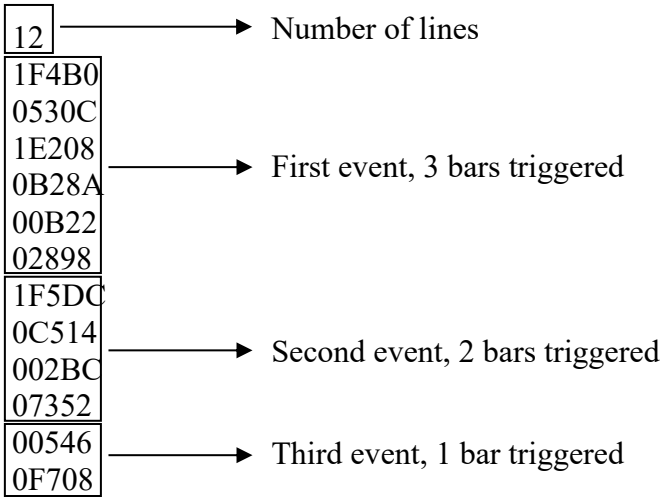
The structure of the configuration file is described below:

- Line 1 indicates the number N of data lines contained in the file with decimal notation.
- Line 2 contains the bar counter information with hexadecimal notation (1F if is the first bar of a multiple event, 0 otherwise) and the Side A energy value for the first bar with hexadecimal notation.
- Line 3 contains the bar address with hexadecimal notation and the Side B energy value for the first bar with hexadecimal notation.
- Line 4, 5, … N:
    - If it is a multiple event lines 2 and 3 are repeated for all the bars in the event.
    - If it is a single event another event can be added to the configuration file.

Follows an example of configuration file that contains 3 events:

- The first event has 3 triggered bars
- The second event has 2 triggered bars
- The third event is a single event

Cfg file	Description
12	Number of data lines in file
1F4B0	Bar counter = 31(1F); Side A energy value = 1200
0530C	Bar address = 5; Side B energy value = 780
1E208	Bar counter = 30(1E); Side A energy value = 520
0B28A	Bar address = 11; Side B energy value = 650
00B22	Bar counter = 0, last bar of the event; Side A energy value = 2850
02898	Bar address = 2; Side B energy value = 2200
1F5DC	Bar counter = 31; Side A energy value = 1500
0C514	Bar address = 12; Side B energy value = 1200
002BC	Bar counter = 0, last bar of the event; Side A energy value = 700
07352	Bar address = 7; Side B energy value = 850
00546	Bar counter = 0, single event; Side A energy value = 1350
0F708	Bar address = 15; Side B energy value = 1800



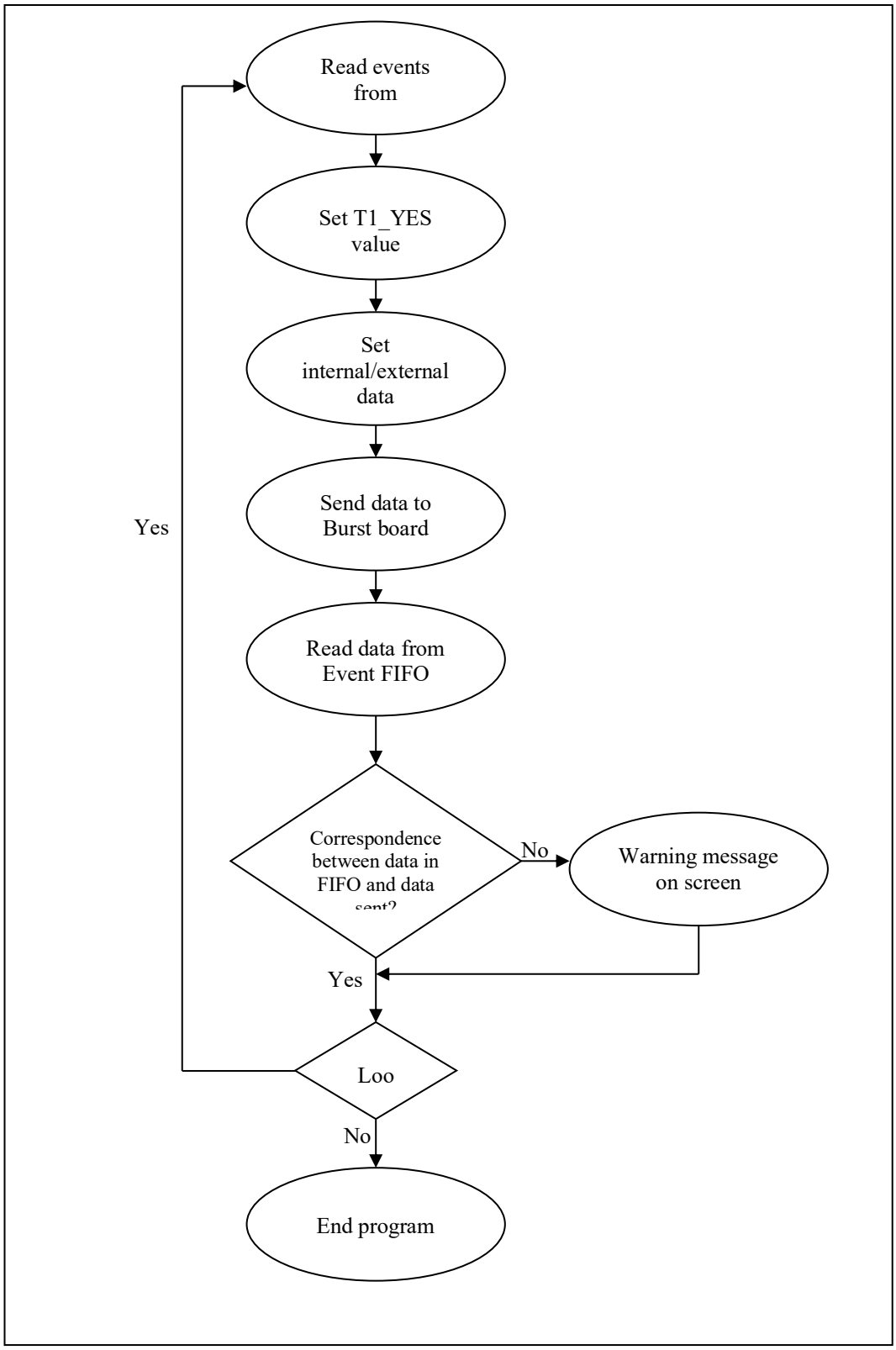


Figure 4-6: Flow chart of software capabilities.

4.5 TIMING DIAGRAMS

In this paragraph are shown the timing diagrams generated by the I/O card on the VME crate in some different cases. The path generated is consequence of the configuration files selected for the test.

Reading points in input to the oscilloscope used to visualize time diagrams are taken from Connector 1 (signals to/from FEE, see Table 3-3) in TTL format, and correspond to:

BRSB_DATA_DW
MRSB_STB_DW
BURST_TIMING
MCAL_CK5_DWN

Signal RESET_N was taken from pin 25 of the Altera Data Handling PLD.

4.5.1 PROVA1.DAT

The following diagram was obtained using Prova1.dat as the configuration file.

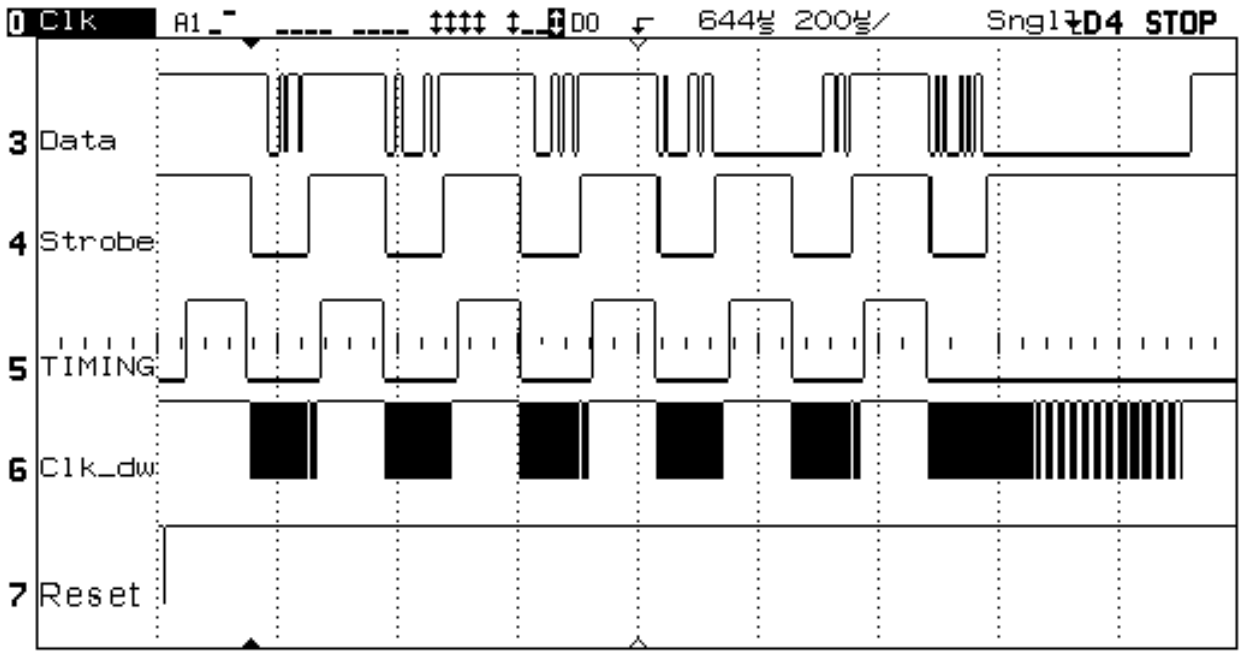


Figure 4-7: Timing diagram obtained using Prova1.dat as the configuration file.

Prova1.dat:

6
1f0bb
03033
1e0dd
040ee
000ed
050ac

4.5.2 PROVA5.DAT

The following diagram was obtained using Prova5.dat as the configuration file.

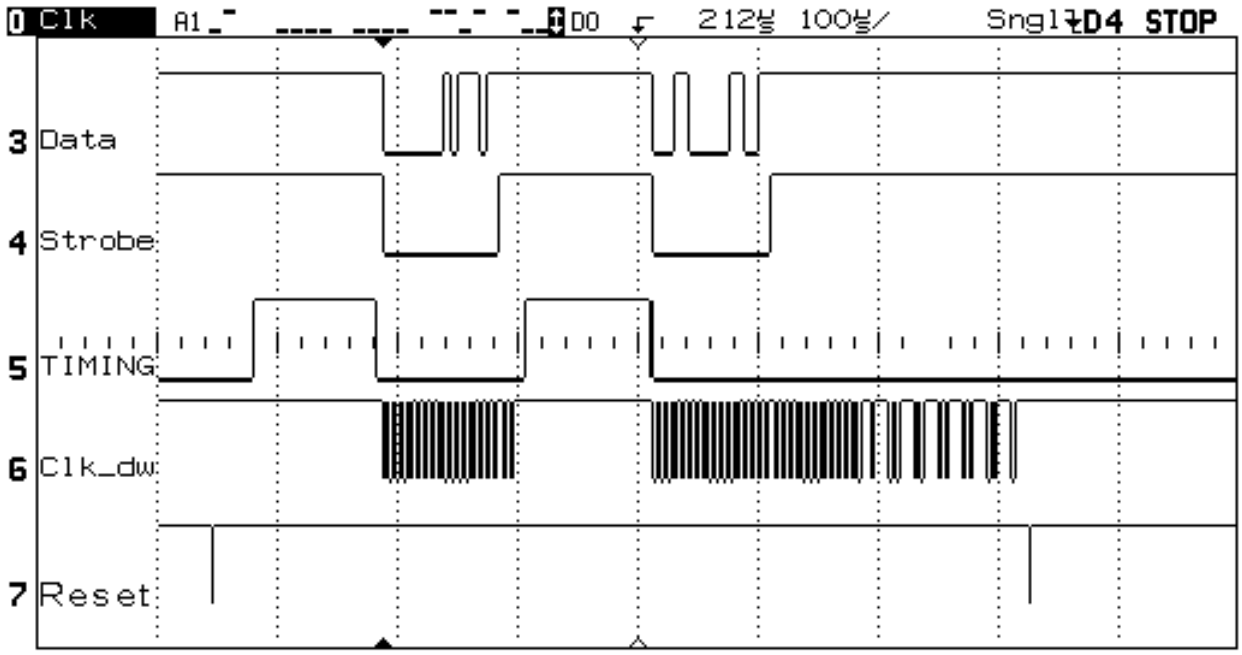


Figure 4-8: Timing diagram obtained using Prova5.dat as the configuration file.

Prova5.dat:

2
000bb
03033

4.5.3 PROVA7.DAT

The following diagram was obtained using Prova7.dat as the configuration file.

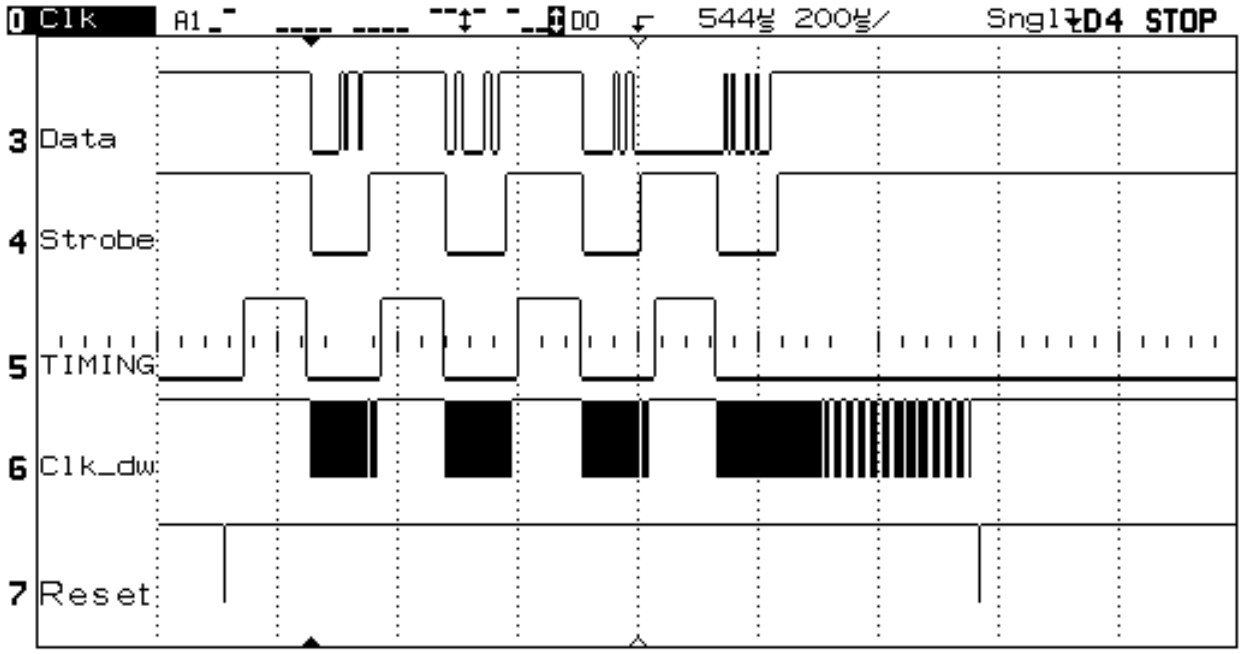


Figure 4-9: Timing diagram obtained using Prova7.dat as the configuration file.

Prova7.dat:

4
000bb
03033
000cc
05123

4.5.4 SINGLE BAR FROM FRONT PANEL

A single bar event can be simulated introducing appropriate data on the front panel of the SW. Follows a timing diagram generated by the event:

00123
12345

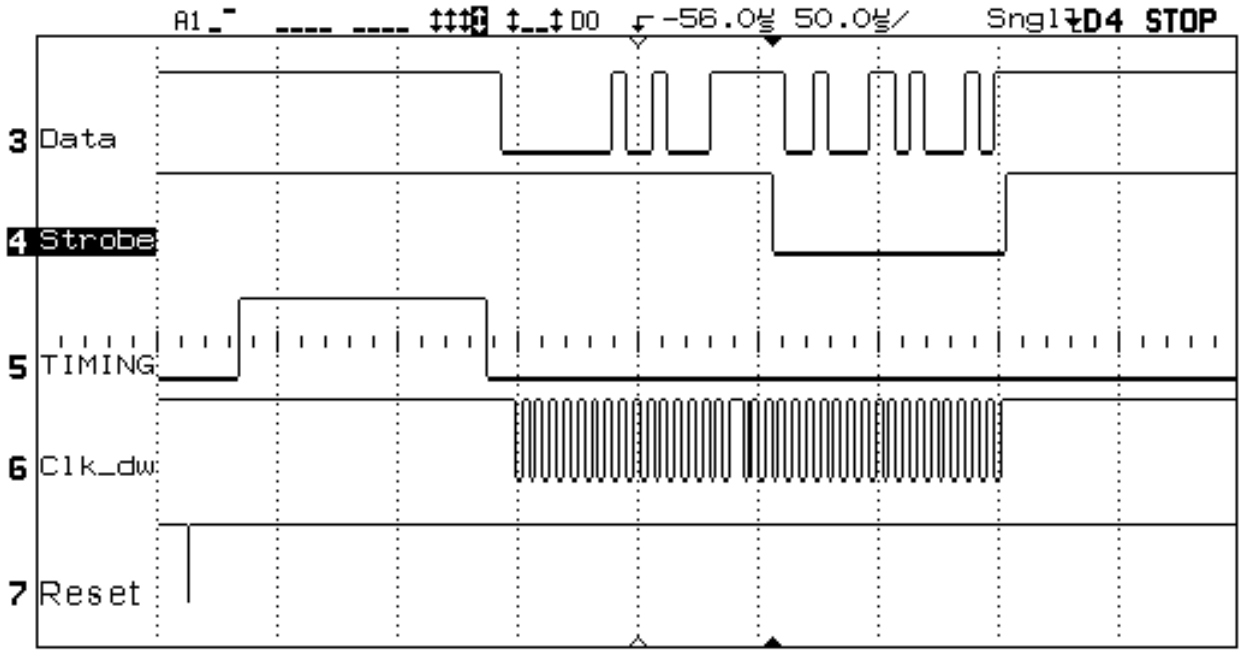


Figure 4-10: Timing diagram obtained using data from front panel.

4.6 TESTS PERFORMED WITH PATTERN GENERATOR

To reproduce more precisely data flow transmitted by FEE, a Pattern Generator (PG) has been used, as simulations performed by the software driven Input/Output VME Card (see par. 3.4) could not reach the 5 MHz clock speed of the FEE.

4.6.1 PULSE GENERATOR SET-UP

Pattern Generator has been connected to the Connector 1 of the Burst board (26 pin), to reproduce data coming from the FEE.
The PG sends four signals to the Burst board:

MCAL_CK5_DWN	5 MHz clock signal; PG starts to generate it before the first Burst Timing signal is sent, and continues until the user gives the stop command on the PG control panel (anyhow after all data is sent).
BRSB_STB_DW	Strobe signal.
BRSB_DATA_DW	Generated data.
BURST_TIMING	Burst timing signal with a duration of 6 clock pulses.

The PG was appositely programmed to give the desired four signals. Clock has been appropriately chosen to give 200 ns of pulse period (5 MHz clock).

The Burst Timing signal is the first signal sent to the board. One Burst Timing signal is sent for each event. After a few clock pulses from Burst Timing signal (corresponding to about 4 μs), data and strobe signals are sent to the board.

The clock signal is sent continuously to the board even after the last data packet is sent, in order to have the bar counter value decrease as events are read from the onboard EVENT FIFO. Should the clock be interrupted before the reading cycle from the Event FIFO ends, the Event counter register would not decrease when events are read causing a wrong behavior of the board.

Two different cases have been simulated with PG:

4.6.2 SIMULATIONS PERFORMED: SINGLE EVENT

A single event has been sent to the burst board, both after a board reset (FIFO empty) and not (FIFO not empty).
In Figure 4-11 is shown the timing diagram of a single event sent when FIFO is empty; the 4 generated signals are shown together with the WRITE_DATA_TO_FIFO (negated) and the FIFO_EMPTY (negated) bits.

The two data words sent where (see RD-2 for the format definition):

00000 000000000001 (in binary form)
10000 000000000001 (in binary form)

That were correctly read as:

- 1 bar to read
- Bar energy side A = 1
- Bar address 16
- Bar energy side B = 1

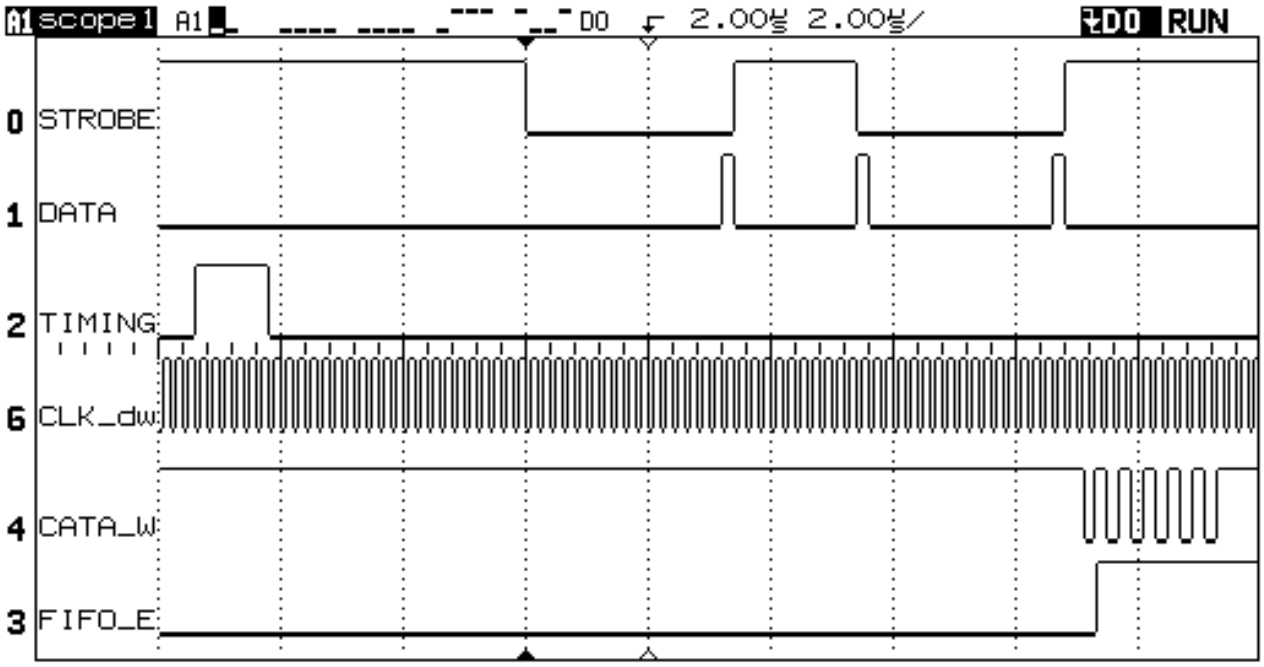


Figure 4-11: Timing diagram showing a single event, the first entering the FIFO after a board reset. DATA_W bit (negate) shows when data is written to the Event FIFO. FIFO Empty bit (negate) raises as data is written in the FIFO.

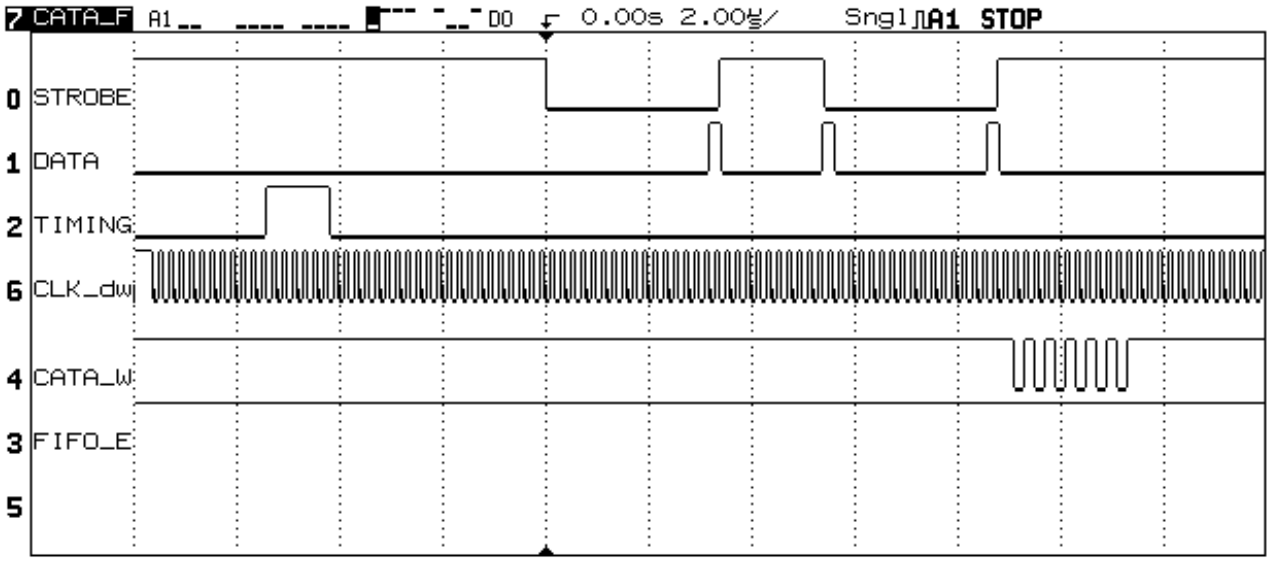


Figure 4-12: Timing diagram showing a single event. FIFO Empty bit (negate) shows that in this case FIFO is not empty, even if Event Counter is 0.

4.6.3 SIMULATIONS PERFORMED: TWO EVENTS

A double event has been sent to the burst board.
In Figure 4-13 is shown the timing diagram of the two subsequent events; the 4 generated signals are shown together with the WRITE_DATA_TO_FIFO (negated) and the FIFO_EMPTY (negated) bits.

- The first was a single event with 1 triggered bar:
  The two data words sent where (see RD-2 for the format definition):
  00000 000000000001 (in binary form)
  10000 000000000001 (in binary form)
  That were correctly read as:
  - 1 bar to read
  - Bar energy side A = 1
  - Bar address 16
  - Bar energy side B = 1
- The second event was constituted of 2 triggered bars:
  The four data words sent where (see RD-2 for the format definition):
  11111 000000000001 (in binary form)
  10000 000000000001 (in binary form)
  00000 000000000001 (in binary form)
  10000 000000000011 (in binary form)
  That were correctly read as:
  - More bars to read
  - Bar 1 energy side A = 1
  - Bar address 16
  - Bar 1 energy side B = 1

- Last bar to read
- Bar 2 energy side A = 1
- Bar address 16
- Bar 2 energy side B = 3

The following timing diagrams show the patterns generated to simulate single events (Figure 4-11 and Figure 4-12) and multiple events (Figure 4-13).

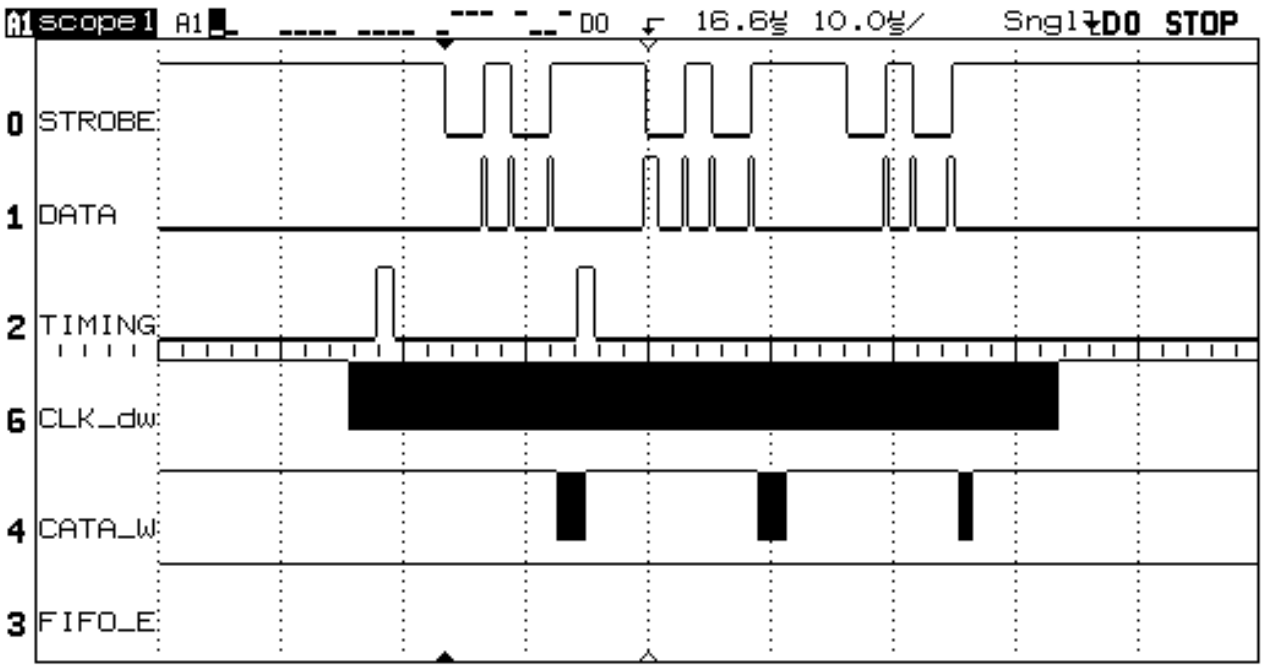


Figure 4-13: Timing diagram showing two subsequent events.

4.6.4 SIMULATIONS PERFORMED: CONCLUSIONS

The Burst board showed to work properly in most situations, with single and multiple events. The only problem found concerns single events:

> When a single event is the first event entering the EVENT FIFO of the Burst board after FIFO has been cleared, the Event Counter doesn't increase. Nevertheless the event is not lost, even if there is no evidence of it when polling the Event Counter Register it is still in the FIFO.
> Subsequent events are stored regularly in the FIFO, and Event Counter after the first event increases correctly.

To put in evidence this problem, the reading routine of the software has been modified in order to poll on the Event Counter Register. The reading process was performed cyclically until the Event Counter Register was returning 0 events in FIFO. A cross check performed on the FIFO EMPTY bit

(PIN 1 on PLD IC11, see electrical schemes) revealed that when the first event enters the FIFO the FIFO EMPTY bit changes state (Figure 4-11), but Event Counter stays 0.
When subsequent events are sent, the event counter increases of 1 step for each event. If data is read until event counter register returns 0, the last event sent to the FIFO is left inside it, and the FIFO_EMPTY bit stays high (FIFO not empty) as shown in Figure 4-12.

5. ENCLOSURES

1. Burst board PCB drawing.
2. Burst board electrical schemes.
3. Burst board registers timing drawings.